COMPARISON OF THREE DIFFERENT CONCEPTS OF HIGH DYNAMIC RANGE AND DEPENDABILITY OPTIMISED CURRENT MEASUREMENT DIGITISERS FOR BEAM LOSS SYSTEMS

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Abstract

Three Different Concepts of High Dynamic Range and Dependability Optimised Current Measurement Digitisers for Beam Loss Systems will be compared on this paper.

The first concept is based on Current to Frequency Conversion, enhanced with an ADC for extending the dynamic range and decreasing the response time. A summary of 3 years' worth of operational experience with such a system for LHC beam loss monitoring will be given. The second principle is based on an Adaptive Current to Frequency Converter implemented in an ASIC. The basic parameters of the circuit are discussed and compared with measurements. Several measures are taken to harden both circuits against single event effects and to make them tolerant for operation in radioactive environments. The third circuit is based on a Fully Differential Integrator for enhanced dynamic range, where laboratory and test installation measurements will be presented. All circuits are designed to avoid any dead time in the acquisition and have reliability and fail safe operational considerations taken into account.

STRUCTURE OF THE COMPARISON

Each concept will be described by means of specifications, implementation and performance. In the conclusion a summary of the three methods will be given.

CURRENT TO FREQUENCY CONVERTER

Specifications

LHC protection requires a high reliability Beam Loss Monitoring system. The Front End card, referred to as the CFC card, has been designed to be exposed to a maximum of 500Gy integrated dose for 20 years LHC life-time.

To achieve a reliability level SIL3 (10^{-7} to 10^{-8} failure/h) of the system, several different test modes, status information, protection circuits and a redundant data transmission are implemented. For the verification, different tests have been performed, such as irradiation, temperature, magnetic field, and burn-in tests.

A summary of the System Specification is given in Table 1.

Table 1: CFC Specifications

Measurement range	2.5pA to 1mA
Error range from 10pA to 1mA	-50% to +100%
Error range from 1nA to 1mA	±25%
Maximum input current	561mA
Minimum acquisition period	40us
Input range with minimum acquisition period	5nA to 1mA
Input voltage peak	1500V @ 100us
Radiation Total Dose	500Gy in 20yr

Implementation

To measure a current over this high dynamic range, a Current to Frequency Converter (CFC – Figure 1) based on the balanced charge integrating techniques, has been chosen. In comparison with other switching techniques, the CFC has the advantage that it is without dead times and with no loss of charges.

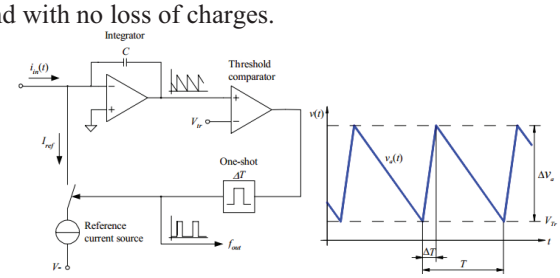

Figure 1: CFC block diagram.

Since the output frequency depends on the input current (where a small current corresponds to a very low frequency), an additional analogue to digital converter (ADC) is added to measure the output voltage of the integrator and to calculate partial counts in the Threshold Comparator card, named BLETC. This measurement decreases the response time and increases the dynamic range. The integration time window of the system is 40µs. The data, including the counted CFC pulses and the integrator output voltage, are transmitted every 40µs to the BLETC. Figure 2 shows the CFC circuit diagram.

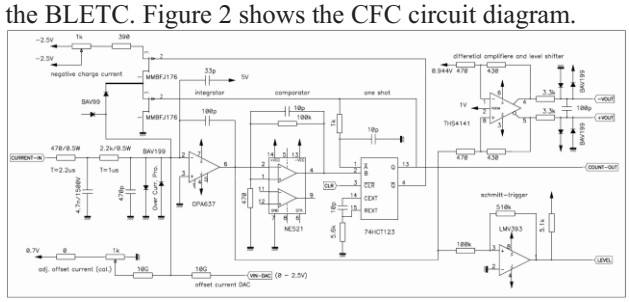

Figure 2: CFC circuit diagram.

To ensure the system is working according to specification and to increase the reliability, several tests, test modes and error detection systems have been added on the CFC card, as shown in Table 2.

Table 2: CFC Tests List

N	Description
1	Before the installation, a calibration and an initial test are performed using a dedicated setup, which performs an

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	automatically generated functional test pattern. This system will also be used for additional tests after tunnel installation.
2	The constantly performed test using 10pA offset current, provides a count every 20s. After absence of the count for more than 120s, an error bit is activated.
3	For the data transmission a CRC is added, which is verified at the BLETC. Due to the redundant link, even if one transmission is corrupted, data are still available.
4	The Card Identification is sent and checked every transmission to ensure the used threshold table belongs to the correct module.
5	Lost data transmission will be detected by the check of the Frame Identification at each data transmission.
6	When the CFC TEST is activated (High Voltage ≥ 1655V for 240s), 100pA are added on the input of the CFC, to test the corresponding response of the acquisition chain. This test is required to be done at least every 24 hours. If not done no beam permit is given.
7	32 status bit are sent and read out every transmission. Depending on the indicated malfunction a beam-dump is initiated.
8	A full maintenance plan has been implemented to guarantee the best performances over the time.

Performance

Approximately 800 CFC cards for a total of 6400 channels have been deployed. In the first 3 years of operation only 2 emergency beam abort requests were issued due to failures that occurred during stable beam conditions. Both failures occurred in the optical link that connects the CFC card in the tunnel to the TC on the surface. In Figure 3 is shown the linearity test executed on the CFC cards:

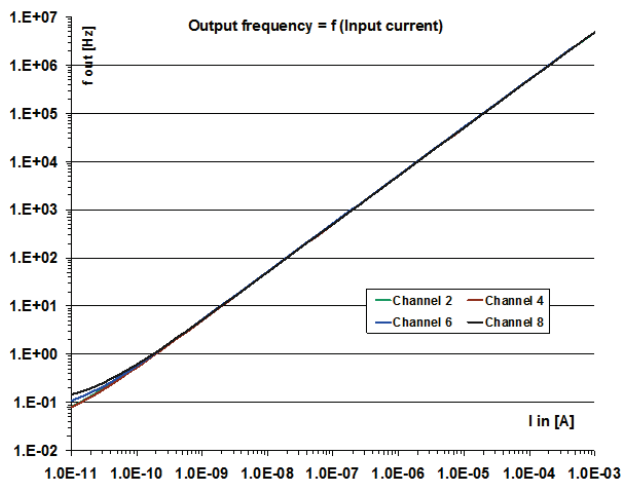

Figure 3: Measurement verification with CFC card.

HIGH-DYNAMIC RANGE RADIATION-TOLERANT ASIC

Specifications

Ionizing Radiation Monitors with different design and operating principle are employed in the BLM system throughout the accelerator chain at CERN. Two general features common to all of the monitors are a current output that spans several orders of magnitude, and the requirement of either front-end electronics able to withstand the radiation effects, or alternatively a cabling infrastructure that carries the signal to a location where the radiation level is not a concern.

In this context a radiation-tolerant Application Specific Integrated Circuit (ASIC) has been developed at CERN, using a commercial 0.25um CMOS technology. The design targets, primarily Ionization Chambers and Diamond Detectors, employed in the BLM system at CERN, are also suitable for different types of current-output monitors, with both single-ended and differential output. The ASIC will allow the user to place the front-end electronics close to the detector, which offers advantageous features: the measurement is carried out in loco so the results are transmitted digitally, reliably, while offering a potentially very low sensitivity to noise and interference, and the minimum input capacitance to the front-end circuit.

Table 3: ASIC Specifications

Measurement range	10pA to 1.05mA
Error	<±10%
Radiation Total Dose	100kGy in 20yr
Minimum acquisition period	40us
Input range with minimum acquisition period	1nA to 1.05mA

Implementation

The circuit topology is based on a charge-balance current-to-frequency converter, taking advantage of its charge-driven operation, introducing multiple selectable quantization steps and a logic system that sets and changes the aforementioned step in the CFC according to the signal level. This provides a fine charge resolution at low input levels and coarse quantization step at higher input levels.

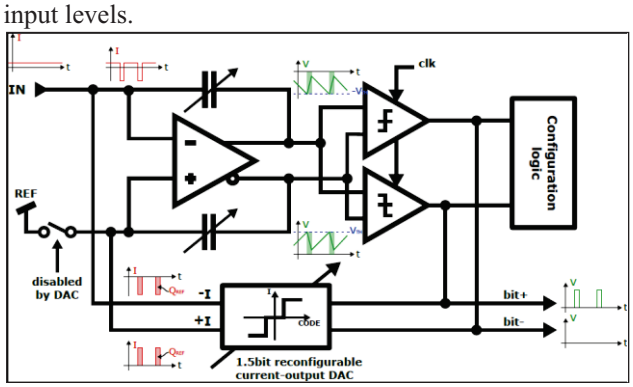

Figure 4: Charge-balance current-to-frequency converter.

The scheme shown in Figure 4 covers the full dynamic range of the input signal. The circuit architecture has been devised in such a way that positive or negative current inputs can be integrated indifferently, without the need for configuration. A signed signal is paired with the conversion code and available to the user.

The conversion reference is embedded on a chip, based on a 1.2 band-gap reference to minimize temperature dependence, and with an optional external resistor for fine calibration of the LSB step.

The ASIC circuit diagram in Figure 5 shows the input and output pin of the ASIC.

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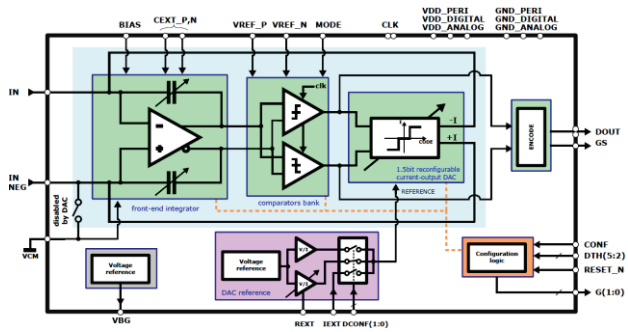

Figure 5: ASIC circuit diagram.

The adaptive mode, as shown in Figure 6, is based on the following concept: the employed charge reference (LSB) depends on the value of the input signal and the charge left in the integrator from the previous conversion.

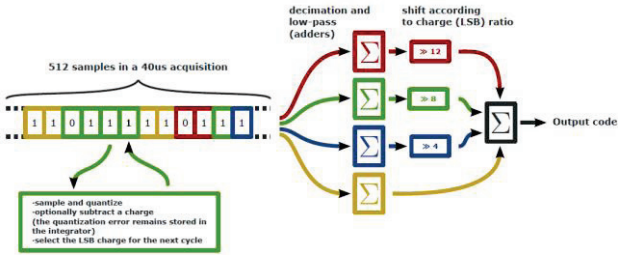

Figure 6: ASIC adaptive range mechanism.

Performance

The first prototype is able to measure the charge collected in 40µs over a six decade range (40fC - 42nC or, equivalently 1nA-1.05mA integrated over 40µs, coupled DC), independently from the detector type and biasing, in environments with ionizing radiation levels up to 100kGy (or 10 Mrad(Si)). For the chips already tested, the charge-to-digital conversion is affected by a linearity error that is within +/-5% (Figure 8), and the reference charge drifts of less than 600ppm/K and of 3% at 10Mrad TID. A second version of this device is planned, with focus on providing a compact solution to be mounted directly on the radiation monitor.

Figure 7 shows the preliminary Linearity performance. Figure 9 shows the ASIC layout.

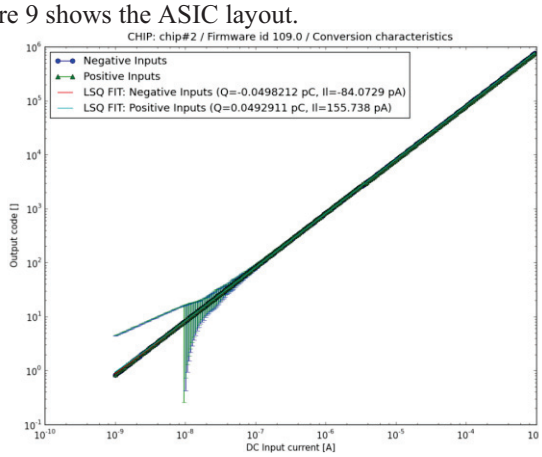

Figure 7: ASIC linearity test.

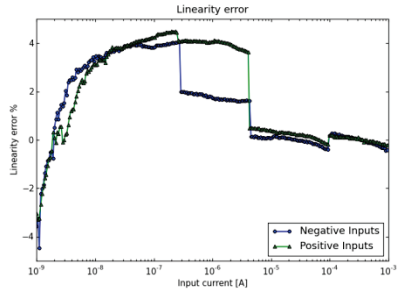

Figure 8: ASIC Linearity Error

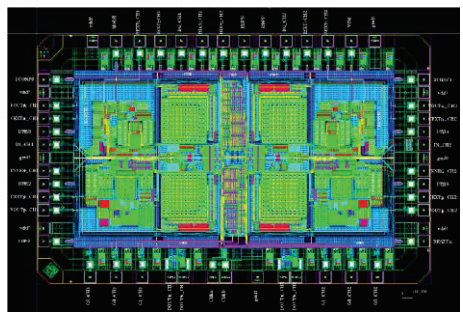

Figure 9: ASIC Layout

FULLY DIFFERENTIAL INTEGRATOR

Specifications

A wide range current digitizer card is needed for the implementation of the acquisition module for Beam Loss Monitoring in CERN Injector complex, which includes: LINAC4, Proton Synchrotron, BOOSTER and their transfer lines. The possibility to connect several detector types with positive or negative input current polarity is required. On the other hand, the electronic will be placed in protected areas and no radiation tolerance is required. The system will be used as monitoring and protection system, therefore a high reliability design is required. Table 3 gives a summary of the main specification for the Fully Differential Integrator design.

Table 3: Fully Differential Integrator Specifications

Measurement range	10pA to 200mA
Error	<±10%
Maximum input current	561mA
Minimum acquisition period	2us
Input range with minimum acquisition period	31nA to 200mA
Input voltage peak	1500V @ 100us

Implementation

To reach such high dynamic range e.g. $2 \cdot 10^{10}$, a mixed measurement technique has been implemented in a new card called BLEDP. This combination of measurement techniques is done by means of a Fully Differential Frequency Converter (FDFC), and a Direct ADC (DADC).

In this way the measurement range is split into two overlapping ranges: the FDFC used between 10pA÷10mA and the DADC between 100µA÷200mA. The front-end automatically switches between the two modes depending on the input current value, as shown in Figure 10.

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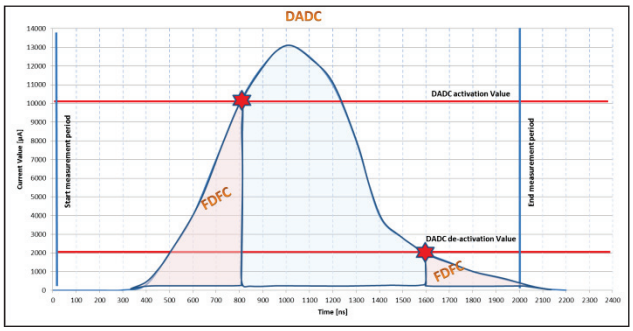

Figure 10: FDFC and DADC functionality.

The FDFC circuitry is based on a fully differential integrator as shown in Figure 11.

A status signal is used to select in which branch of the fully deferential stage the input current is integrated.

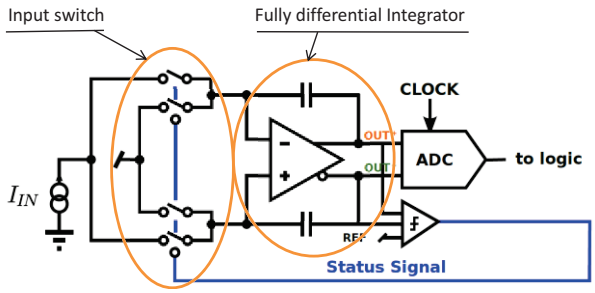

Figure 11: Fully differential integrator block diagram.

Two comparators are used to check the deferential output voltage against a threshold. Whenever the limit is exceeded, the status signal toggles to the complementary value (from 0 to 1 or from 1 to 0) and the input current is integrated in the other branch. This functionality is shown in Figure 12.

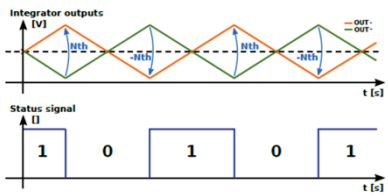

Figure 12: Fully differential integrator functionality.

A block diagram describing the implementation of the complete digitisation circuitry is shown in Figure 13.

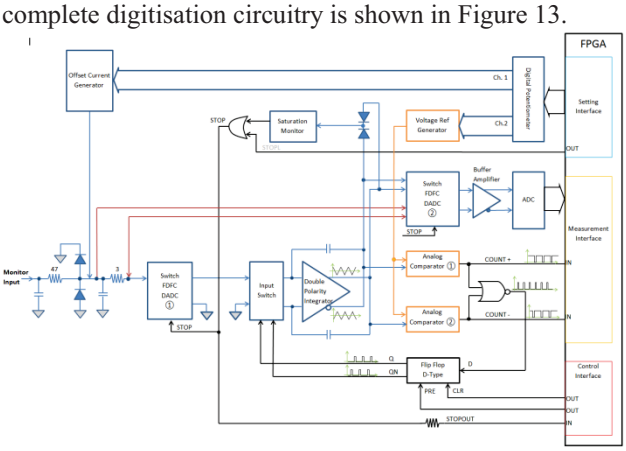

Figure 13: Block diagram of the digitisation circuitry.

By default mode of operation, the current input coming from the monitor flows through the Switch n.1 and the Input Switch into the Double Polarity Integrator (DPI), which is designed with a very high gain and input impedance. Two discrete comparators with a threshold settable by the FPGA are used to drive the Input Switch and to give the "Count" information to the FPGA.

The Switch n.2 routes the output of the DPI into a 16bit ADC – 10MSPS, through a Buffer Amplifier that includes a 3th order filter.

The readout current from the FDFC circuitry is created with a combination of Counts using an ADC with a resolution of 24 bits [4]. Whenever the input current value exceeds the "DADC Activation Value", the DADC circuit is activated by means of the STOP signal. In this way, the input current is routed by the Switch n.1 to the ground, and the voltage dropped on a 3 ohm resistor is routed by the Switch n.2 to the ADC. In the meantime the FDFC circuitry is reset. If the current input falls below "DADC De-Activation Value", switches n.1 and n.2 are released and the measurement mode is again reconfigured as FDFC.

The Power Supply Structure of the BLEDP card is designed to prevent the failure propagation from an input channel to the main control. A main $48V_{DC}$ input is routed through the backplane into the BLEDP module. Local power supplies are used to supply the circuitry. Finally two circuit breakers decouple groups of 4 channels, as shown in Figure 14.

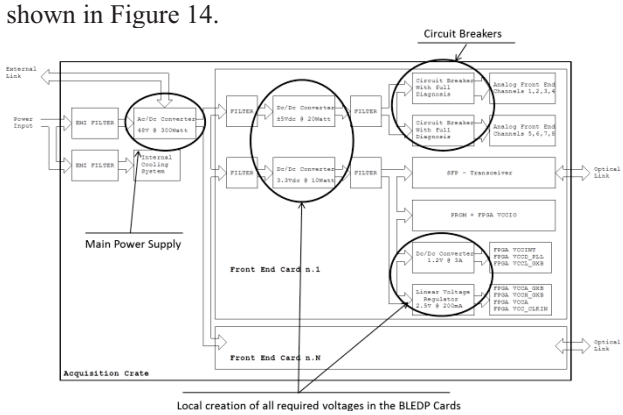

Figure 14: BLEDP power supply structure.

The BLEDP card has 8 input channels. The result of their digitization is transmitted by optical link to the BLETC card through an SFP module. During the test phase there is the possibility to plug in the BLEDP an SFP Ethernet module for the data transmission by Ethernet. Numerous Status information signals are collected by the BLEDP and sent out, to guarantee the full diagnosis of the system.

The optimization of the current leakage and the noise reduction requires a special 12 layer Printed Circuit Board (PCB) design.

The PCB layout architecture allows the total separation between the digital and the analog part from noise and crosstalk. A picture of the BLEDP module can be found in Figure 15.

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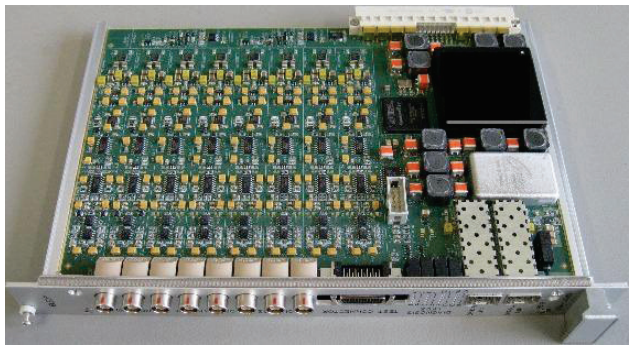

Figure 15: BLEDP card.

Performance

The BLEDP card is still under development. Several preliminary tests in the laboratory and in the CERN PS accelerator have given very good feedback.

Several sensors such as: IC (Ionization Chamber), BLMD (Diamond Detector), LIC (Little Ionization Chamber at 0.4bar pressure), SEM (Secondary Emission Monitor), PEPII (Cherenkov Monitor) have been connected to the inputs of the card, collecting signals that are well correlated with accelerator losses.

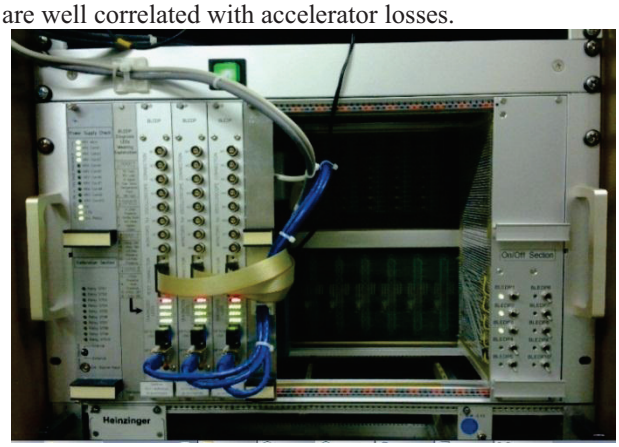

Figure 16: Full crate in the PS test installation.

To verify the FDFC and DADC measurement capability, a preliminary Linearity Test has been performed as shown in Figure 17.

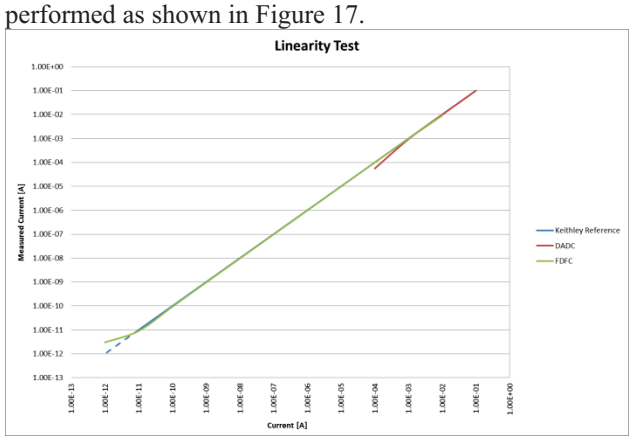

Figure 17: FDFC and DADC linearity test.

The Measurement Error is below 10% in all the full range. The possible selection of the FDFC and DADC thresholds are visible in Figure 18.

Figure 18: FDFC and DADC error.

CONCLUSIONS

A comparison of the available solutions for CERN Beam Loss Monitors is given in Table 4.

The CFC card guarantees a tested and reliable solution for the immediate usage, but with increasing accelerator energy, new solutions are needed.

The Radiation Tolerant ASIC and the Fully Differential Integrator should cover the entire scenario in terms of Input Monitors with different characteristics and installation in several accelerators.

Table 4: Solution Comparison

Solution	**CFC**	**ASIC**	**BLEDP**
Input Polarity	Positive	Positive and Negative	Positive and Negative
Operating Input Range	2.5pA to 1mA	300pA to 1.05mA	10pA to 200mA
Error	±25%	±10%	±10%
Sensitivity	1pA	10pA	2pA
Minimum Acquisition Period	40us	40us	2us
Input range with minimum Acquisition Period	5nA to 1mA	1nA to 1.05mA	31nA to 200mA
Radiation Tolerance	500Gy in 20yr	100kGy in 20yr	Not Tested
Availability	Production	Developing	Developing

The Sensitivity is measured considering an offset input current, and 10sec as measurement period.

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