FAST ORBIT FEEDBACK CALCULATION IMPLEMENTATION FOR TPS

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Abstract

Fast orbit feedback (FOFB) application is planned for the Taiwan Photon Source (TPS) at storage ring commissioning. Part of the application is transferred to the beam position electronics which implements global orbit position data concentration, its processing and actuating the magnet power supply controllers via optical links. The beam position electronics (Libera Brilliance+) includes gigabit data exchange (GDX) modules with Virtex6 field programmable gate array. The feedback calculation algorithm is based on the SVD – the PI controller will be applied in the modal space for individual eigenmodes. The calculation will be distributed to all GDX modules to reduce overall latency. Each GDX module will calculate either 4 vertical or 4 horizontal magnet corrections.

This article presents details about the FOFB topology and implementation in the GDX module.

SYSTEM OVERVIEW

The TPS storage ring will use a 24-cell DBA lattice and will have 24 straight sections for insertion devices, six of them 12 m-long and 18 of them 7 m-long. It will be a combined-function magnets lattice structure with 10 nm rad emittance and will be located in the inner tunnel of the TPS storage ring [1].

The Libera Brilliance+ instrument is a beam position processor instrument used in the TPS. It provides wide and narrow bandwidth data paths with excellent measurement and stability capabilities [2]. The fast orbit feedback capability (FOFB) is provided by an extension module – the Gigabit Data Exchange (GDX) module. The GDX module is tightly connected with its neighbour BPM and TIM modules and receives fast position data streams over Low-voltage Differential Signalling (LVDS) links to ensure low latency [3].

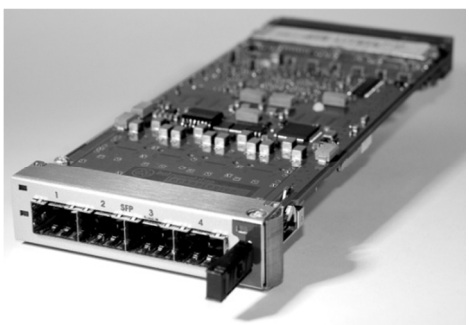

Figure 1: The Gigabit Data eXchange module.

The module contains Virtex6 field programmable gate array (FPGA) with TPS custom-made FOFB application. There is also 1 GB of DDR3 available as a circular buffer for the fast data.

CONTROL TOPOLOGY

The Libera Brilliance+ instruments are daisy-chained with fibre optic or copper cables to form a single group of 168 BPMs installed in 48 chassis (see Figure 2). Each instrument runs the EPICS IOC and communicates over GbE network interface to the Control System. The FOFB application runs in the FPGA in the GDX modules. FOFB related parameters are controlled by Libera BASE, running in the Libera Brilliance+.

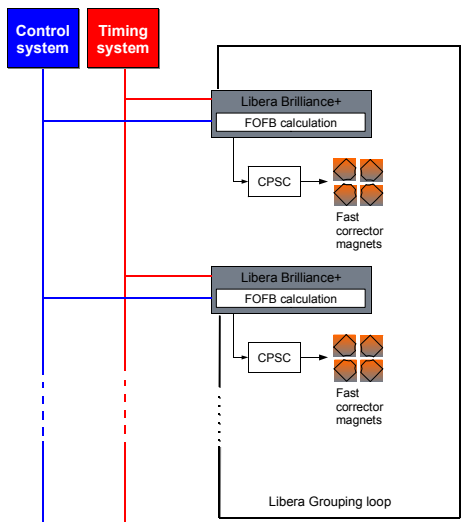

Figure 2: Global control topology.

There are 8 fast corrector magnets located in each of the cells: 4 for the horizontal and 4 for the vertical direction. Fast corrector magnets are controlled by a Corrector Power Supply Controller (CPSC) device which features 2 optical inputs (SFPs) and 8 analogue outputs (20 bit) [4]. Each cell contains 2 Libera Brilliance+ instruments with 3 or 4 BPM modules and 1 GDX module. One Libera Brilliance+ calculates and outputs the data for one set of the fast corrector magnets only (either horizontal or vertical). See Figure 2 for more details.

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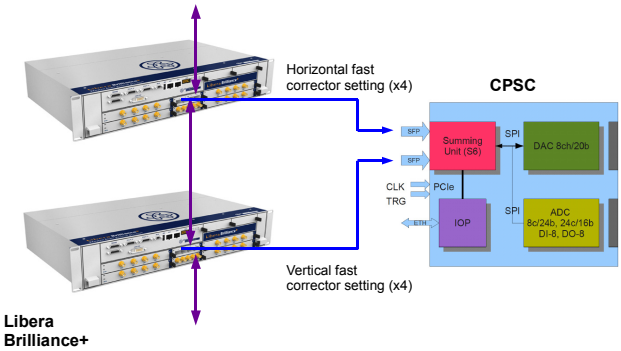

Figure 2: Local control topology.

The global orbit data is present in each GDX module and can be output via UDP/IP as a data stream.

IMPLEMENTATION

The source of the fast orbit feedback look is the beam position data stream with 10 ksamples/second data rate. The data stream is lead from the BPM modules over LVDS connections to the GDX module. The data content after the data concentration includes horizontal and vertical positions (X, Y), SUM and status. The Libera Grouping communicates with its neighbours over two Small form-factor pluggable transceivers (SFPs) at 6.5 Gbps bitrate. It concentrates the source data from all daisy-chained instruments and forms global orbit data. The design includes a measurement of the time needed to concentrate all BPM data. This time can be interpreted as the Libera Grouping latency. The global orbit data packet is then immediately output to a dedicated GbE link which is configured for UDP/IP at 1 Gbps. Due to standard protocols used, the orbit data stream can be received with a standard Windows or Linux based PC with compatible network interface (GbE, support for jumbo frame).

Further down the matrix multiplication scheme (Figure 4), the orbit data is compared to the golden orbit (reference orbit) and its diff enters the matrix multiplication block. The transform matrix from orbit reading to magnet correction is:

$$M_{cx1} = V_{cxe} . PI_{ex1} (S^{-1}_{mxn} . U^{T}_{nxn} . dP_{nx1}) \qquad (1)$$

The position delta (dP) is first multiplied with almost diagonal matrix of singular values ($S^{-1}.U^{T}$) which transforms the data from BPM to eigenmode space. The PI controllers are applied to the multiplication result. In the end, multiplication with the V matrix transforms the data from the eigenmode space to the corrector magnet space and selects which magnet correction is sent to the output.

The multiplication scheme is flexible in terms of the number of BPMs, magnets and eigenmodes. It can output corrections for all magnets or just for local ones. The selection is done with a dedicated filter which in the end equips data packets with corresponding magnet IDs. The magnet correction output is sent through the SFP1, which is configured for AURORA at 2.5 Gbps.

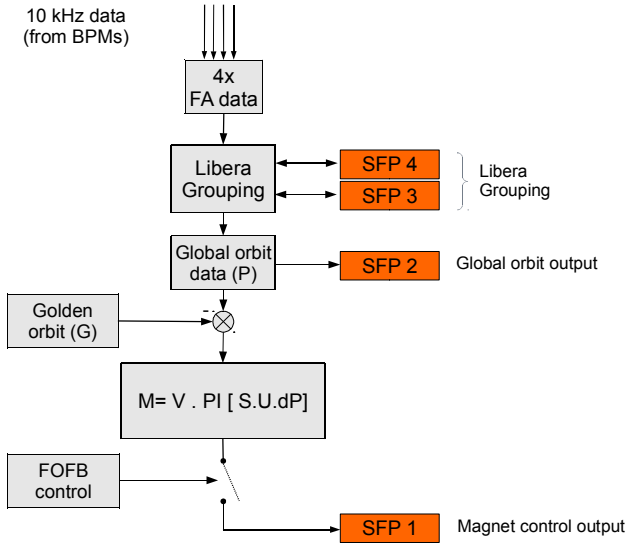

Figure 4: Implementation scheme.

Such approach requires several multiplications of big matrices (up to 128 x 256) but it is designed to do all multiplications in parallel. This was done to reduce the calculation to minimum possible extent. It is estimated that the calculation latency is 2 µs at maximum number of elements and approximately 1.5 µs for the TPS storage ring configuration (96 x 168).

The multipliers used are 18 x 25 bits. The design contains several checkpoints that detect saturation after critical multiplication steps. Whenever necessary, bit width is narrowed to fit multipliers.

Control over matrices is fully supported by the EPICS IOC as well as all the parameter settings.

PRELIMINARY RESULTS AND OUTLOOK

The main driver of the implementation in the FPGA was the overall latency, which consists of a Libera Grouping latency and FOFB calculation latency as the two main contributors. The Libera Grouping latency was pushed to the limits with the use of 6.5 Gbps bitrate in the SFPs and optimization of the Libera Grouping block. Preliminary tests show the Libera Grouping latency of about 50 ns per BPM (not including transmission time over cables around the storage ring). The matrix multiplication block was optimized for the XC6VLX240T chip. Its 768 DSP48E1 slices allow multiplications in parallel thus reducing the calculation latency to minimum (below 2 µs).

Additional reduction of the overall latency was achieved by calculating a single direction per GDX (horizontal or vertical). This reduction is almost negligible compared to the overall latency, however.

First installation at NSRRC will be done in October 2012 and will include software and FPGA upgrade of the

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Libera Brilliance+ instruments. Beam tests are foreseen in the existing TLS booster ring. Besides the general configuration and test of the Libera Grouping functionality, the compatibility test with the CPSC will be performed. Fine tuning will be done on-site with adjustment of bit cutting, to allow for optimal use of multipliers' dynamic range, transform-matrix-elements normalization and fitting the calculated values to corrector magnets.

CONCLUSION

The FOFB implementation has been customized specifically for the TPS. The decision for the high performance Virtex6 chip was correct because it offers flexibility in the design and high performance operation. Preliminary tests showed excellent results for the overall latency and the system will be tested on a larger scale during Autumn/Winter 2012.

Installation and system integration of the TPS accelerator systems is scheduled in 2013. Commissioning will be performed in 2014. FOFB is planned to test at early commissioning phase. Operational FOFB is expected from day one of user service.

REFERENCES

[1] TPS Design Handbook, version 16, June 2009.
[2] Libera Brilliance+ documentation, http://www.i-tech.si
[3] GDX Module Specifications, http://www.i-tech.si
[4] CPSC module Specifications, http://www.d-tacq.com

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