DATA ACQUISITION SYSTEM OF BEAM LOSS MONITORS OF THE J-PARC MAIN RING

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Abstract

Beam loss monitors (BLM) are essential diagnostic devices for the operation of the J-PARC Main Ring, which aims at the acceleration of the world-highest-power proton beams. The data acquisition system of the beam loss monitors is required to measure the time structure of the output signal integrated during the acceleration cycle. The repetition rate of the measurement in the duration needs to reach at a level of tens of Hertz with time jitters less than a few milliseconds. In addition, the measured data must be accessible by the EPICS-based control system, which manages the whole accelerator control. In order to satisfy the requirement, a new type of Input / Output Controller (IOC), which runs Linux on a CPU module of FA-M3 Programmable Logic Controller (PLC), has been adopted. To execute the data acquisition, the CPU module functions with high speed data acquisition modules of FA-M3 on the same PLC-bus. We found that the IOC meets the requirements and the development and maintenance of the software for the IOC is considerably efficient.

INTRODUCTION

BLM of the J-PARC Main Ring consists of 316 pieces of gas chambers distributed along the Main Ring, an injection line and two extraction lines. The output signals from the gas chambers are integrated by a dedicated circuit during the operation cycle of the Main Ring. The data acquisition system of the BLM is required to read the integrated signals tens of times during the cycle to investigate the time structure of the beam loss, as well as the spatial distribution along the accelerators.

A PLC based data acquisition system had been designed and used for the BLM with ordinary sequence CPU modules. However we replaced the ordinary sequence CPUs with F3RP61 CPUs for performance improvement and easier maintenance of the application software.

In the next section, we describe former sequence CPU-based data acquisition system and the following the third section describes latest F3RP61-based data acquisition system.

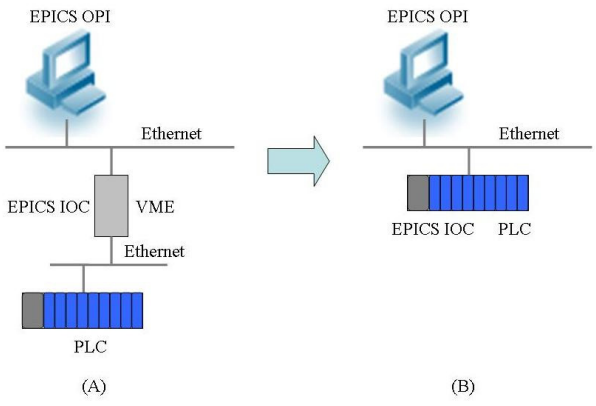

Figure 1: DAQ system configuration.

LADDER-BASED DAQ SYSTEM

Configuration of Data Acquisition System

Figure 1 (A) shows the configuration with the ordinary sequence CPU module. The PLC reads the integrated signal by using the high speed data acquisition module (F3HA08-0N) and transfers the data to a VME computer. A total of 316 signals from the beam loss monitors are assigned to 8 unit of PLC system. The maximum signal per PLC unit is 48. In Figure 1 (A), the VME computer executes the IOC core program so that the operator interface (OPI) can access the acquired data via Channel Access over the Ethernet.

Figure 2 shows the PLC module configuration in Figure 1 (A).

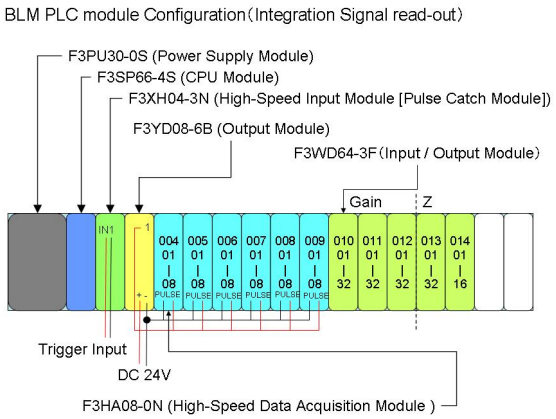

Figure 2: PLC modules of DAQ system.

Sequence of Data Acquisition

In order to measure the time structure of the beam loss during an acceleration cycle at each measurement point, i.e., a gas chamber, PLC repeats the measurement a few tens of times with specified intervals as shown in Figure 3.

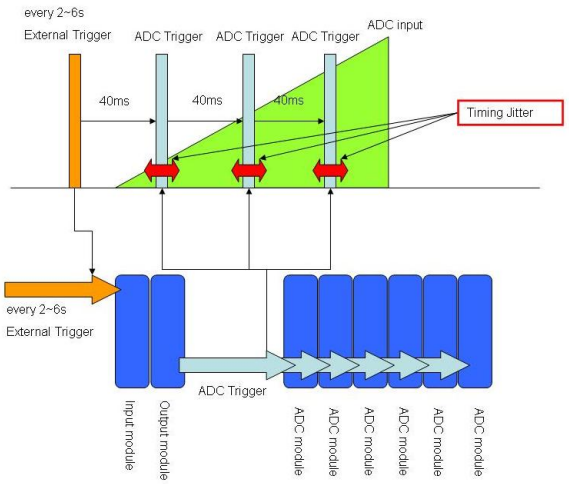

Figure 3: The sequence of data acquisition.

An external trigger goes into a channel of the pulse catch module (F3XH04-3N) to make it interrupt the CPU. When interrupted, the CPU executes an interrupt service routine of the ladder program to activate a sensor control block (SCB), which generates the precise intervals between the measurements. The SCB, which is executed with a constant period, keeps counting the number of scans until the specified interval passes. When the timing to collect data comes, the CPU turns on a output relay of the digital output module (F3YD08-6B) to trigger AD conversion of the high speed data collection modules (F3HA08-0N). After a series of data collection sequence finishes, the PLC system stands by until the next external trigger to come in.

Operational Experiences

The system composed of PLCs and a VME computer had been used for about half a year since May 2008 when the J-PARC Main Ring commissioning started. From the experience during this run, some problem was found. First, the ladder program on the sequence CPU was too complicated to maintain from the following reasons. The ladder program used special and complicated instructions which was not so common, such as SCB to generate the accurate timing signal and the network communication instructions. They made the program hard to read. Second, as show in Figure 1(A), since the process to collect the data was divided into PLC and IOC, it was difficult to find the cause when we find some problem. Trouble shooting took a long time to investigate whether the trouble was in IOC side or PLC side or network communication side.

F3RP61-BASED DAQ SYSTEM

Ease of Maintenance

To solve these problems, a new CPU, F3RP61, was adapted to replace a sequence CPU module. Since F3RP61 runs Linux as its OS, the EPICS core program can run on it to make the PLC itself an IOC. Figure 1(B) shows the system based on F3RP61. All of the PLC's I/O modules of PLC except CPU module remained unchanged in the new system. While the program to process the data was separated into PLC-side and IOC-side in the former system shown in Figure 1(A), both sides are unified into one to be handled by the F3RP61-based IOC as shown Figure 1(B). This simplification improved the system in the following points. First, replacing the ladder programs with a device support specialized in this purpose allowed us more detailed control in the data acquisition procedure. Second, the reliability of the data transfer was improved because data was transformed on the PLC bus instead of Ethernet. Third, trouble shooting became easier since the process was concentrated on F3RP61's IOC. The photo of the system is Figure 4.

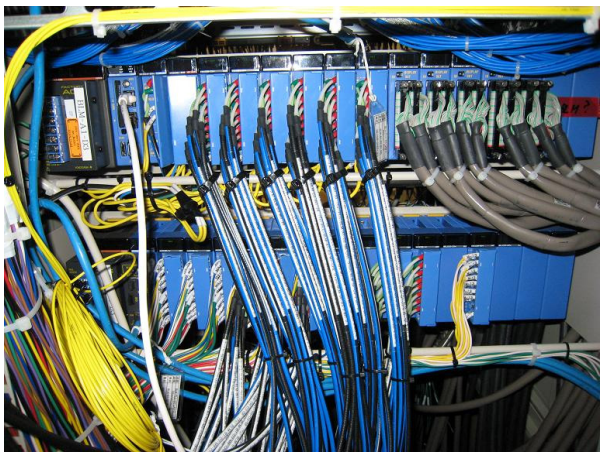

Figure 4: The PLC module of Beam Loss Monitors.

Timing Jitter Measurement

Though simplification of the system by adapting F3RP61 has many merits, the timing jitter in data acquisition has to be carefully considered. While the timing jitter of the data acquisition can not make less than the minimum scan time of SCB (400 micro seconds) on the ordinary sequence CPU module, it is guaranteed that the jitter can not be larger than the scan time. On the other

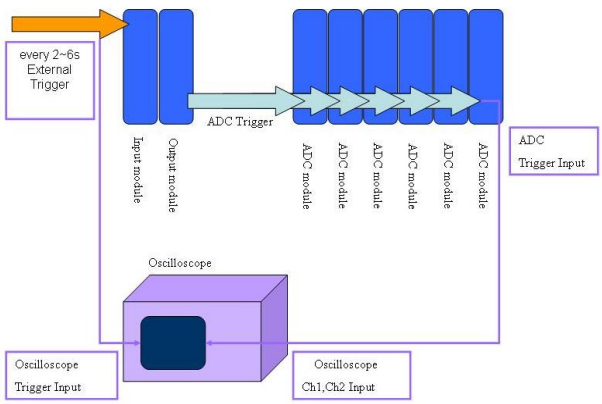

Figure 5: Timing jitter measurement.

hand, the data acquisition with F3RP61 has the latency which is caused by unpredictable real time responsiveness of Linux kernel. A certain level of real time responsiveness is expected on F3RP61 since pre-emption of kernel 2.6 is effective. Because it is not easy to estimate the latency, we measured it by using the setup same as the real system as show in Figure 5.

In this measurement, the jitter of the first output pulse to trigger the high speed data acquisition modules is in reference to the external trigger which was measured by using oscilloscope.

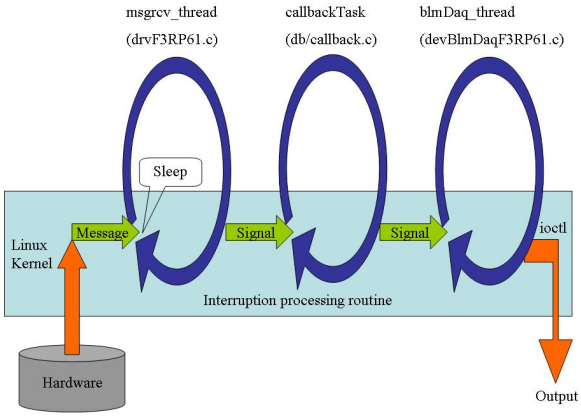

Figure 6: Thread in interruption processing routine.

Figure 6 shows the whole activity that takes place on the CPU in the process from the input to the output. First an interrupt service routine runs in the Linux kernel. The kernel transforms the interrupt into a message to wake up a user thread. A thread spawned in the driver support of F3RP61 receives the message. Then it issues a request to have a callbacktask, an EPICS general purpose thread, process the record waiting for the interrupt. Finally as a result of the record processing, a thread created in a device support dedicated to data acquisition runs to turn on the output relay. This roundabout implementation is a consequence of having utilized existing software as mach as possible to reduce the development work at the cost of performance reduction.

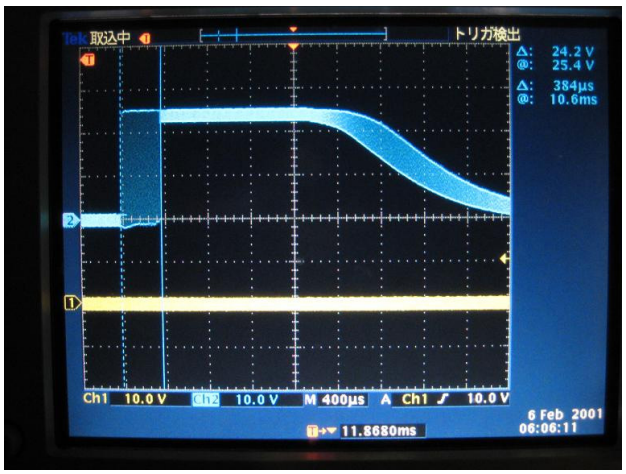

Figure 7: The timing jitter of output signal.

The result of the jitter measurement is shown in Figure 7. The timing jitter measured, for a 15 hour test at a repetition rate of 100 Hz, was less than about 390 micro seconds, which is the as small as that is expected when ordinary sequence CPU module is used. In this measurement, EPICS base was built without enabling priority-based scheduling. In addition, the IOC core process was not made memory resident. In order to confirm that the jitter arose from the latency of the kernel level scheduling, we executed the same measurement with enabling priority-based scheduling and making IOC core memory resident. The result showed that those changes did not make essential difference to indicate that the cause of the jitter was in the Linux kernel. No additional load programs were being executed throughout the measurement.

Result of Operation

The system with F3RP61 has been operated stably during the period from April 2009 to July 2009 of the Main Ring operation, before 2009 summer shutdown.

CONCLUSION

The data acquisition system of Beam loss monitors of the J-PARC Main Ring is updated with F3RP61. Because the core program of EPICS is executed on the PLC unit which runs data acquisition, the hardware structure is simplified and the maintenance becomes simpler. The timing jitter of data acquisition is measured and the timing jitter is not larger than the expected value with ordinary sequence CPU module. The system with F3RP61 has been operated stably during the period from April 2009 to July 2009 of the Main Ring operation, before 2009 summer shutdown.

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