Table 11-5 3U VME64x Signal Field Definitions

	Address Phase 1	Address Phase 2	Address Phase 3	Data Phase
AM[5:0]	0x21	0x21	0x21	0x21
A[7:0]	XAM Code (Table 11-3)	Internal Address A[7:0]	Reserved	D[23:16]
A[15:8]	Device Address A[15:8]	Beat Count	Reserved	D[31:24]
A[23:16]	Device Address A[23:16]	A[23:21] = 0 A[20:16] = GA of Master	Reserved	Reserved
D[7:0]	Device Address A[31:24]	D[7:0] = Subunit number in Master	Reserved	D[7:0]
D[15:8]	Device Address A[39:32] (= 0 for A32)	Reserved	Reserved	D[15:8]

Table 11-6 2eVME Specific Timing Parameters

Timing Parameter	Description	Source (ns)	Destination (ns)
S1	Address and data setup time	-5 min	-11 min
S2	RESP* to DTACK*/BERR* setup time	35 min	10 min
H1	Address or Data hold time	5 min	5 min
T1	Handshake delay time	0 min	0 min

Table 11-7 VME64 Timing Parameters
(From VME64 Standard - Informative Only)

Timing Parameter	Description	At MASTER (ns)	At SLAVE (ns)
4	IACK*, AM[5:0], & Address valid to AS* assertion setup time	35 min	10
6	Time from DTACK* high to time data lines can be driven by MASTER	0 min	0 min
7	Delay time from data line release to MASTER assertion of DS1* (begin Data Phase)	0 min	0 min
8	Data line setup time to DS0*/DS1*	35 min	10 min
10	Delay time from AS* to first assertion of DS0*/DS1*	0 min	-10 min
12	WRITE* valid to DS0*/DS1* setup time	35 min	10 min
16	IACK* and AM[5:0] hold time from last assertion of DTACK* or BERR*	0 min	0 min
18A	AS* negation time from last DTACK* or BERR*	0 min	0 min
23	WRITE* hold time from last negation of DS0*/DS1*	10 min	0 min
26	Delay from first assertion of DS1* to SLAVE assertion of data lines	0 min	0 min
31	Delay from data line release until SLAVE can drive/release DTACK* or BERR* at end of read data phase	0 min	0 min

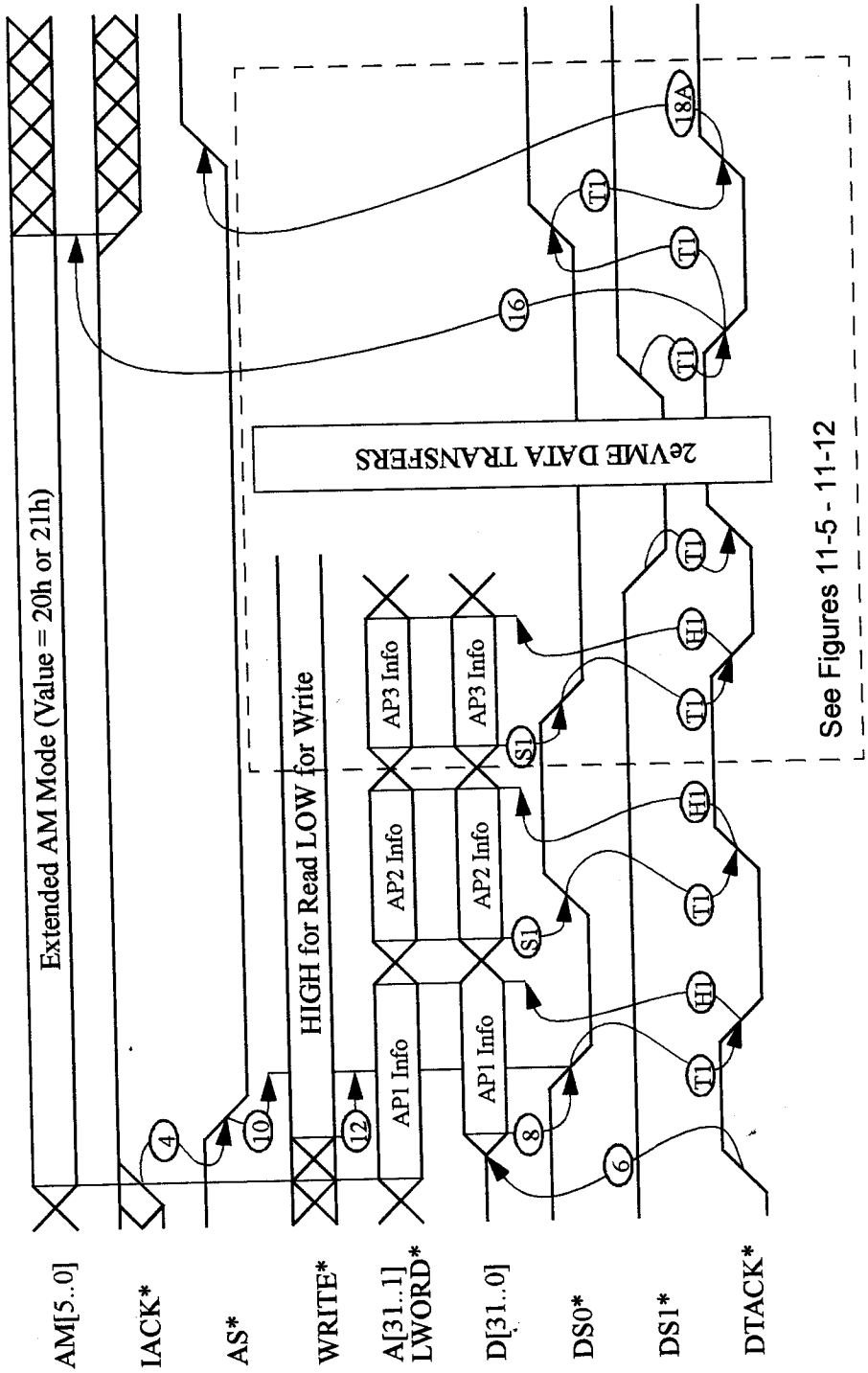

Figure 11-1 2eVME Address Broadcast

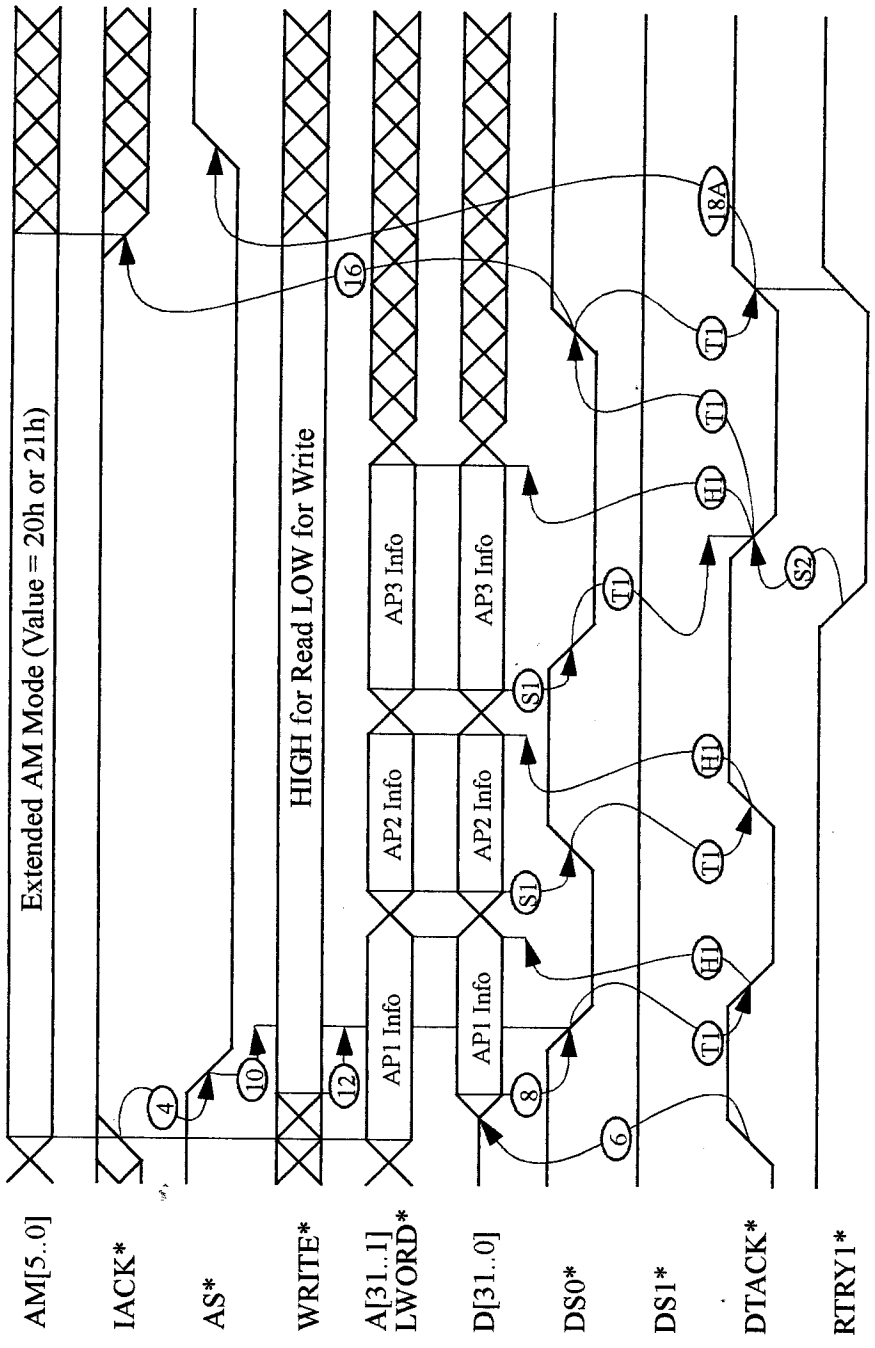

Figure 11-2 2eVME Address Broadcast - Slave Suspend Response

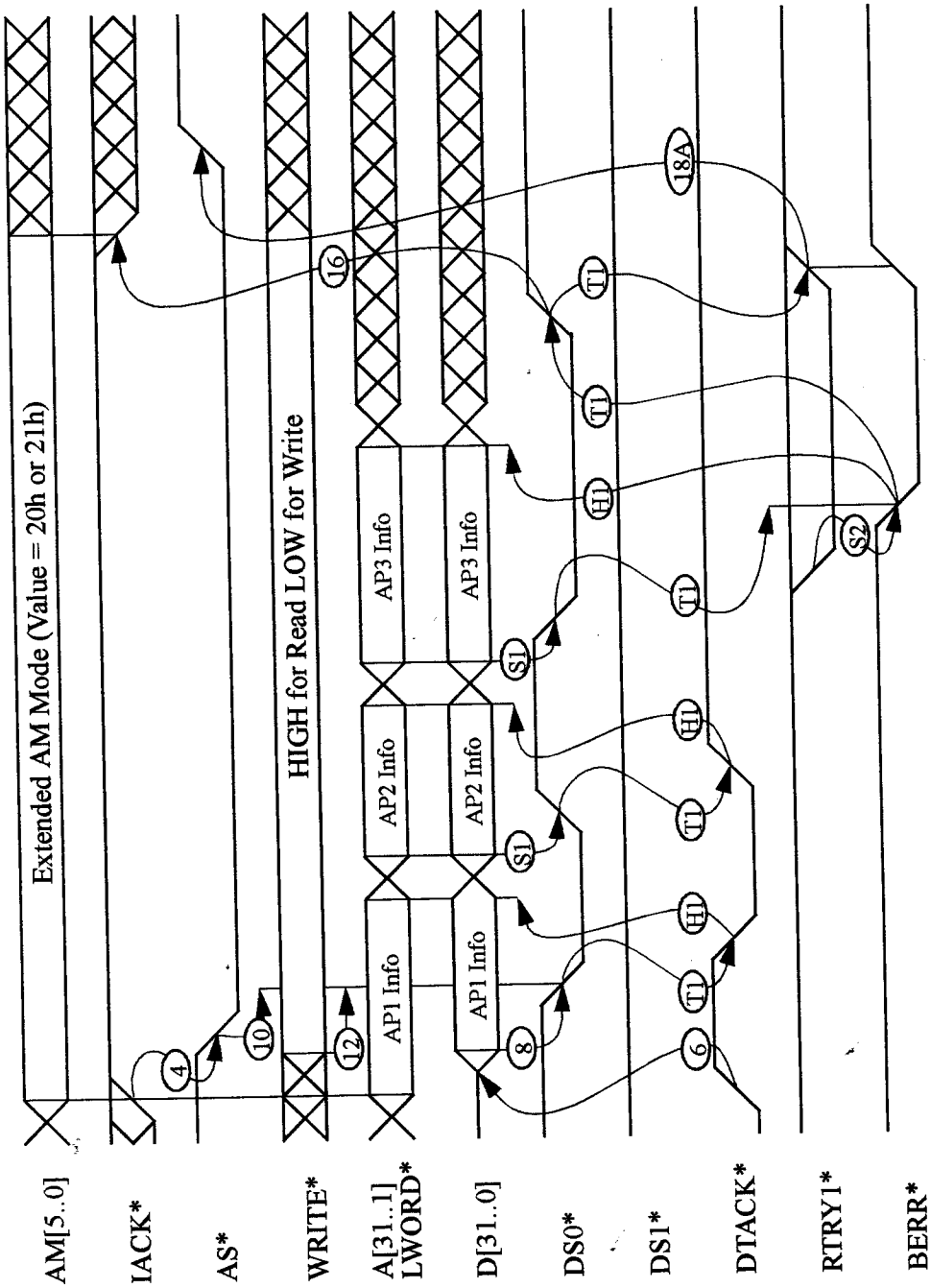

Figure 11-3 2eVME Address Broadcast - Slave Terminated/Error Response

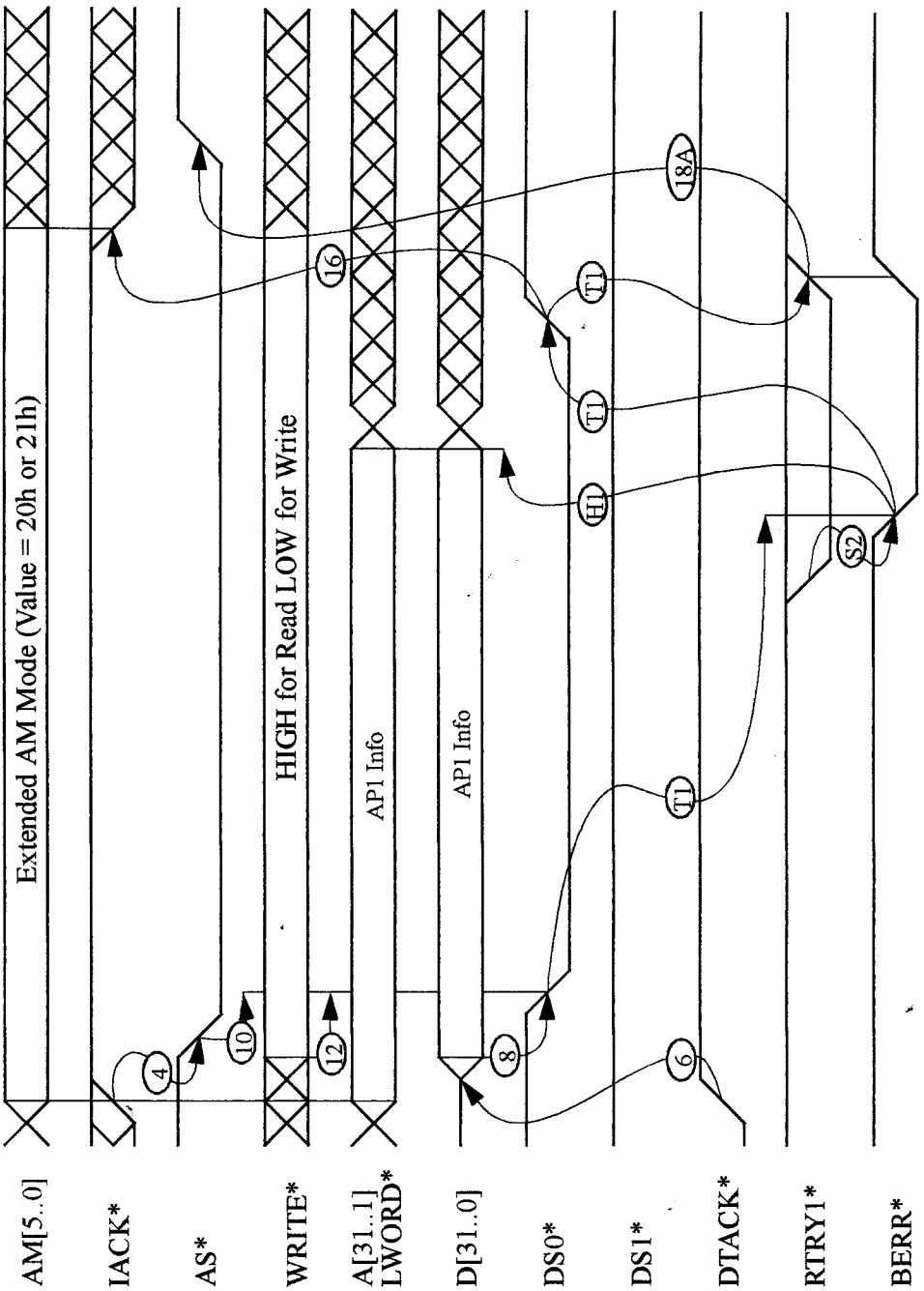

Figure 11-4 2eVME Address Broadcast - Slave Suspend/Terminated/Error Response

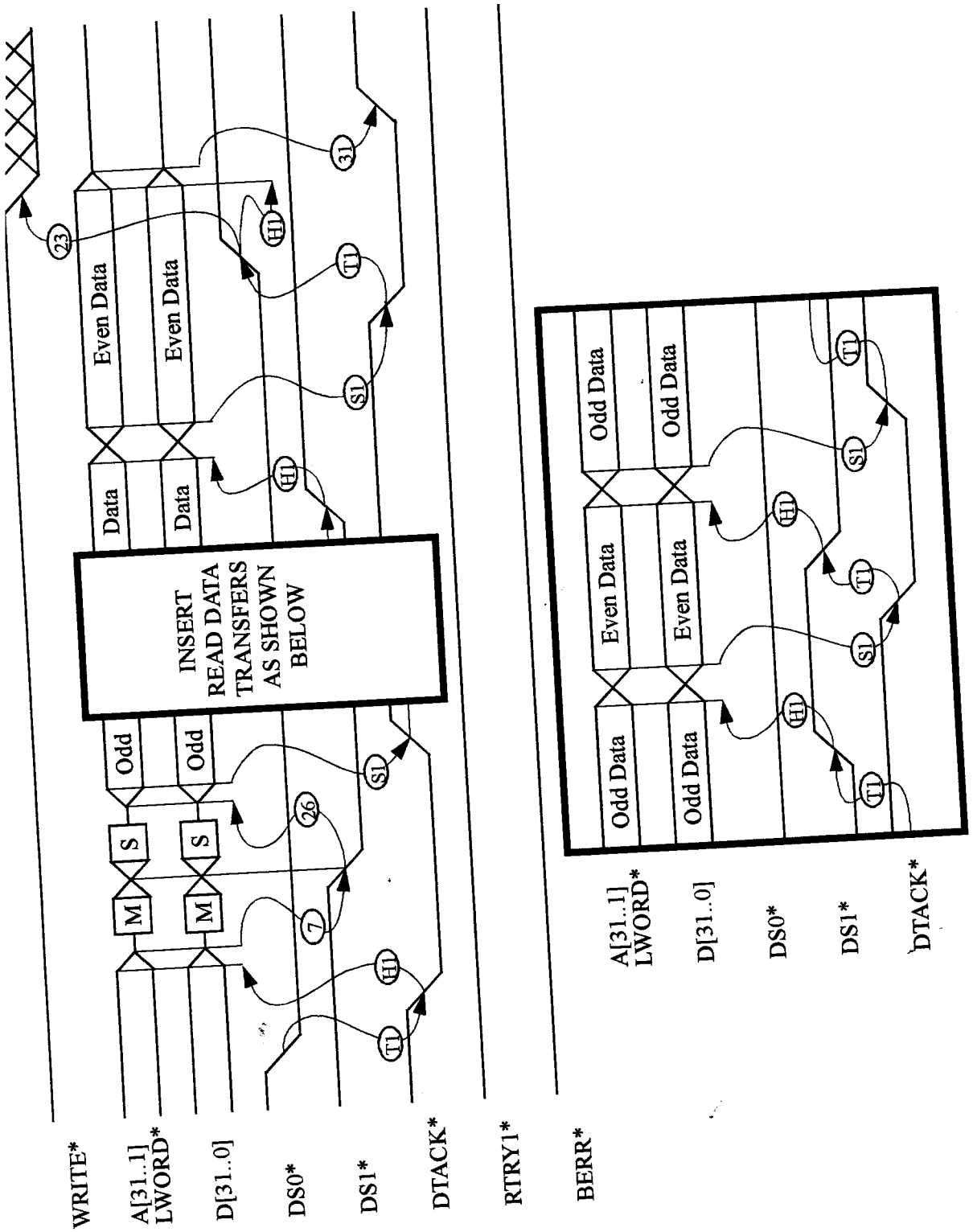

Figure 11-5 2eVME Read Data Transfers - Master Termination

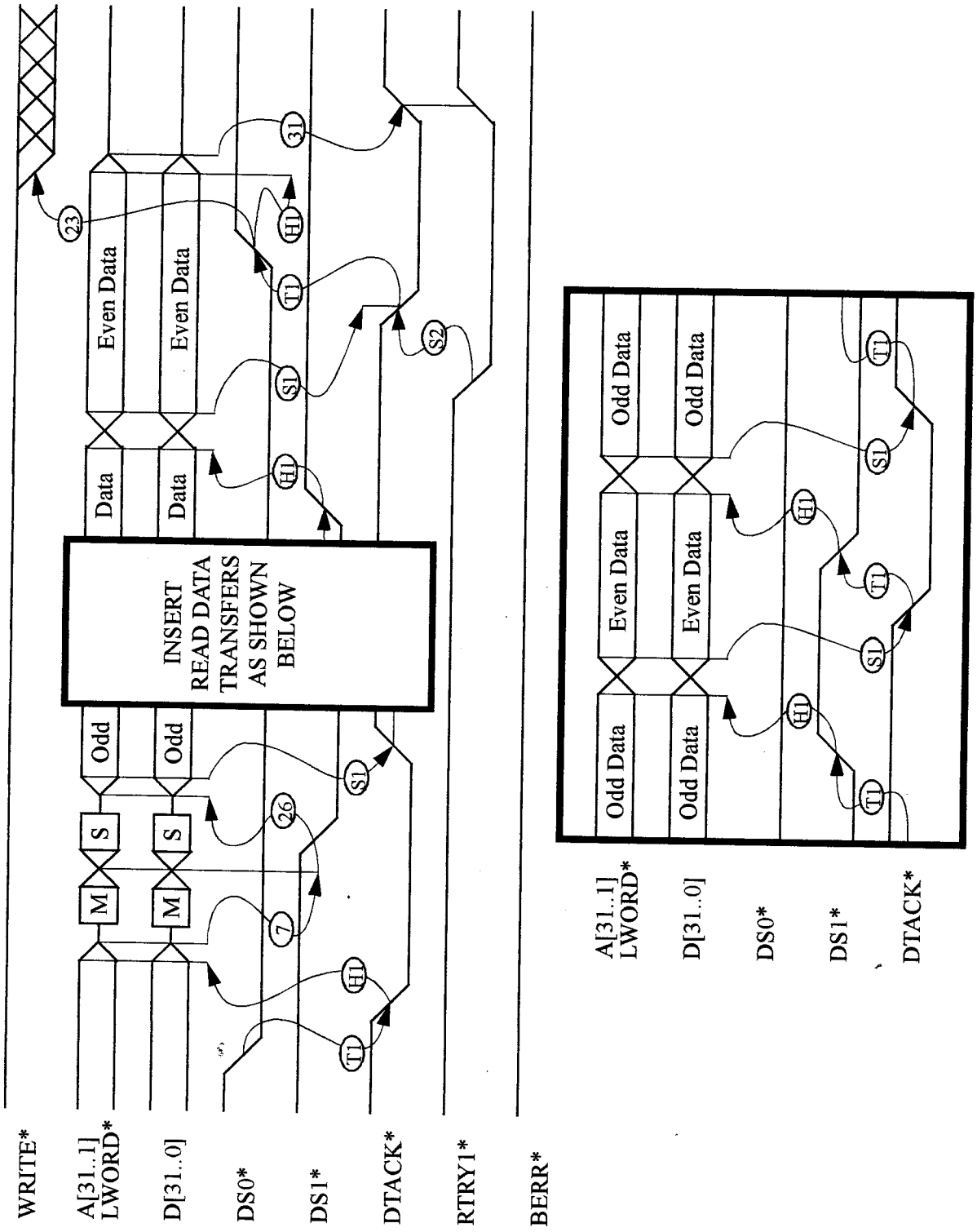

Figure 11-6 2eVME Read Data Transfers - Slave Suspend

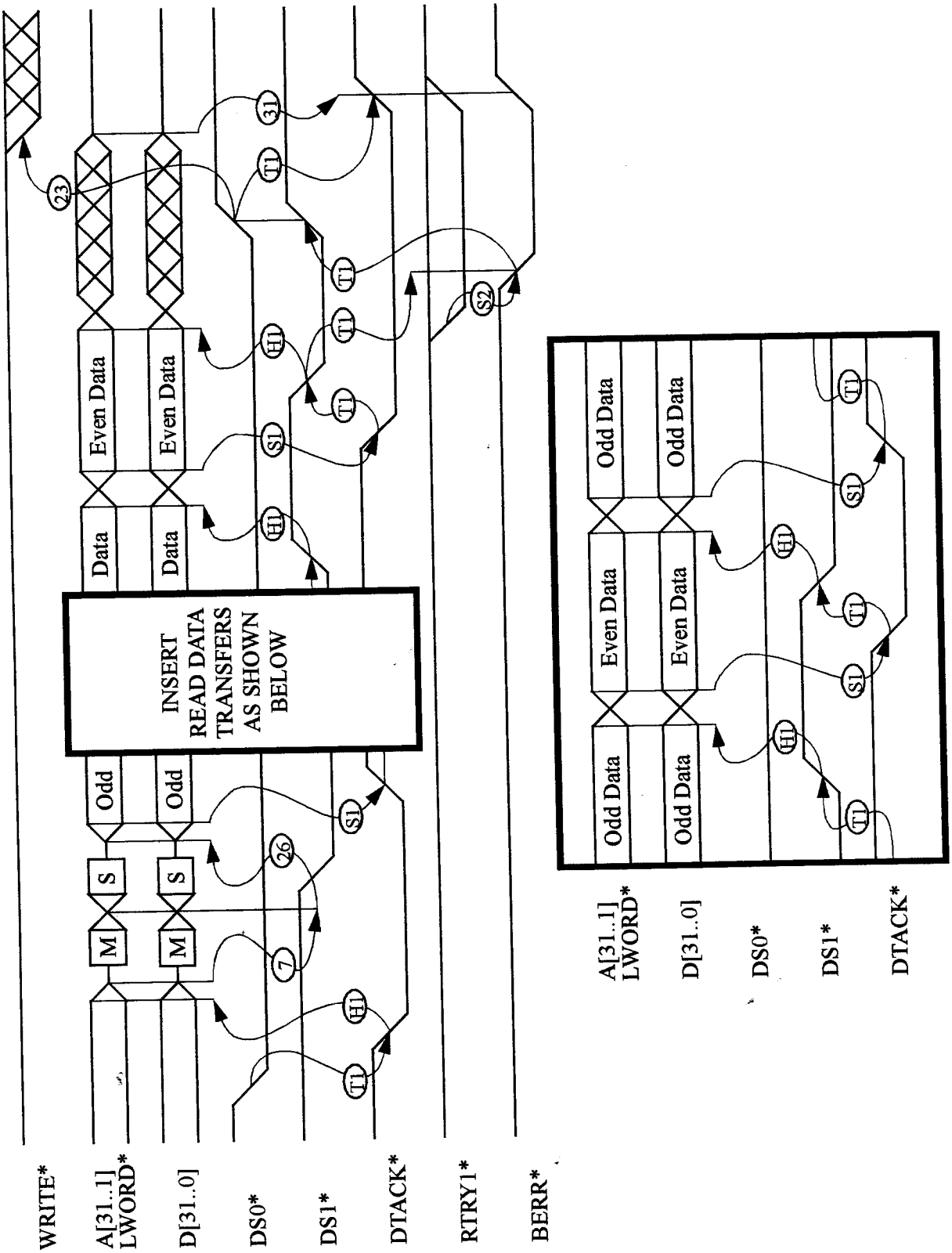

Figure 11-7 2eVME Read Data Transfers - Slave Terminated/Error on Odd Beat

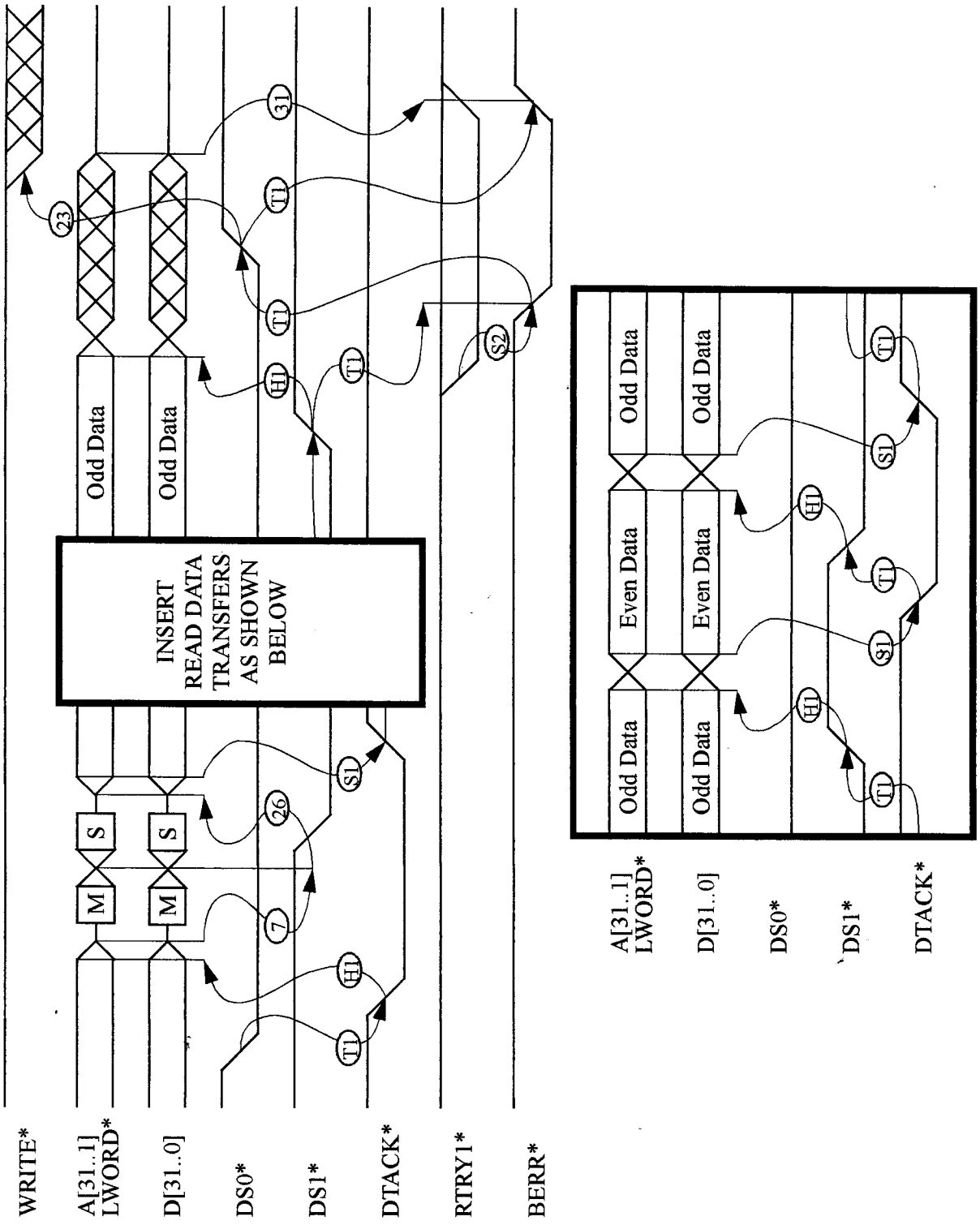

Figure 11-8 2eVME Read Data Transfers - Slave Terminated/Error on Even Beat

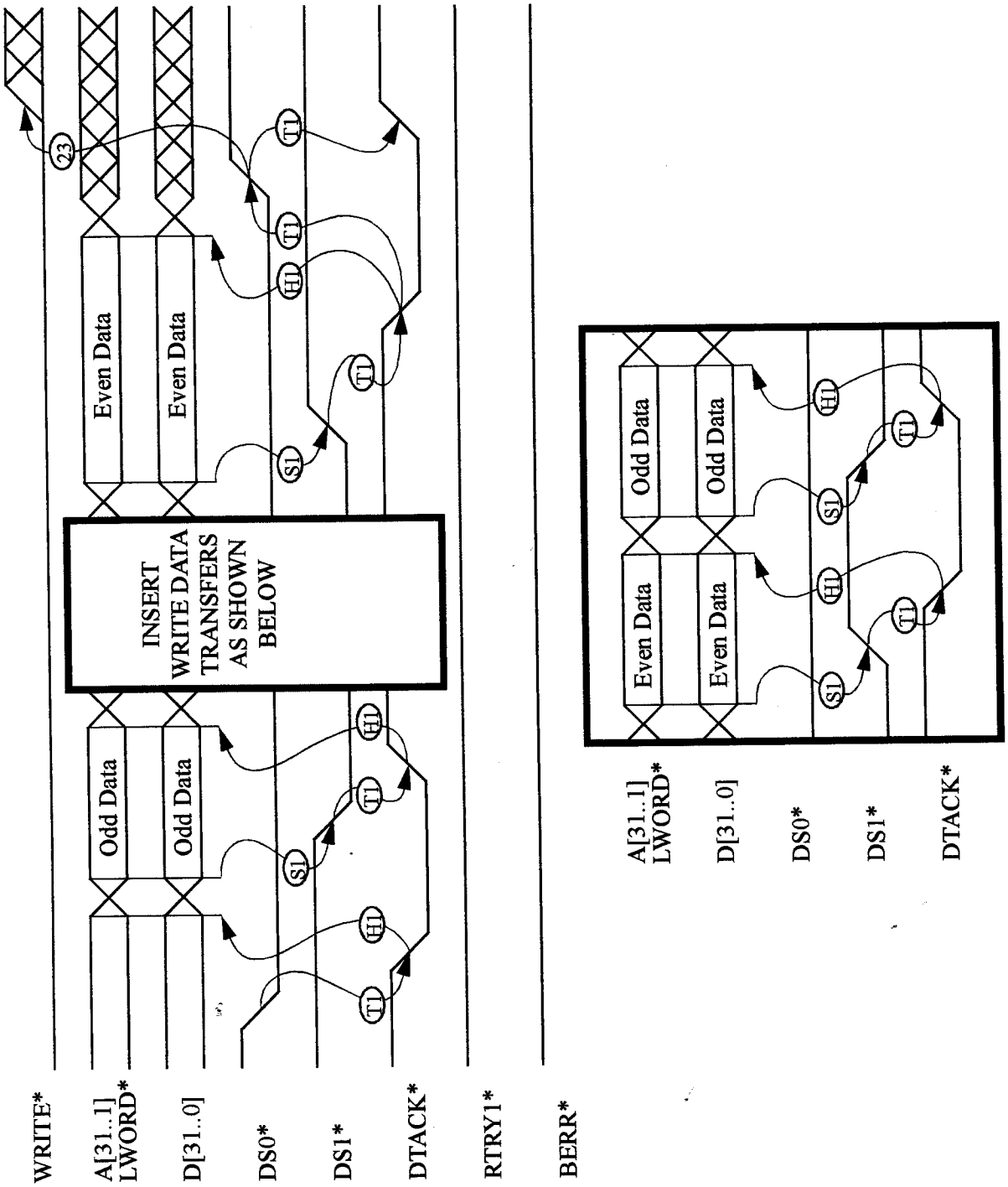

Figure 11-9 2eVME Write Data Transfers - Master Termination

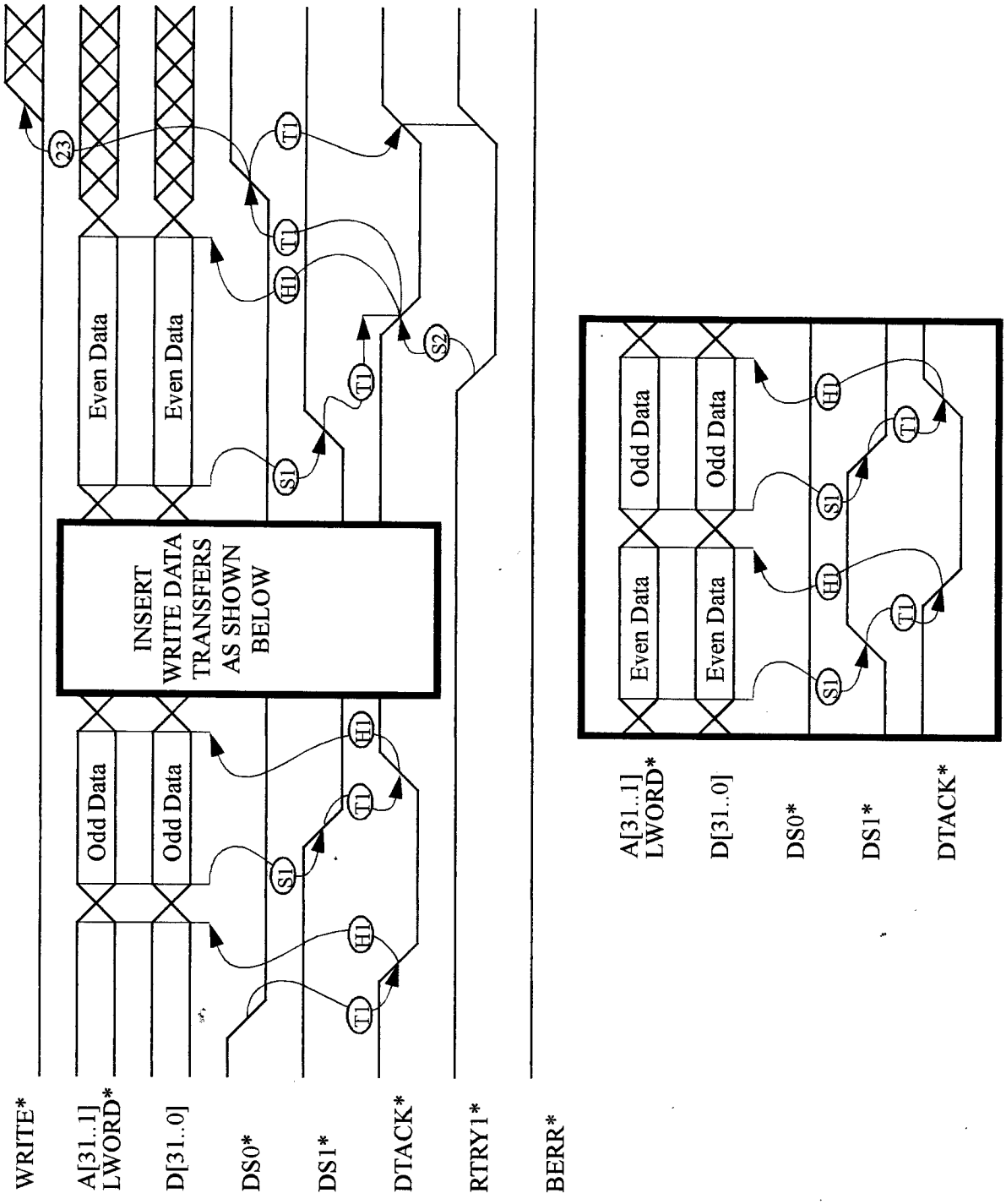

Figure 11-10 2eVME Write Data Transfers - Slave Suspend

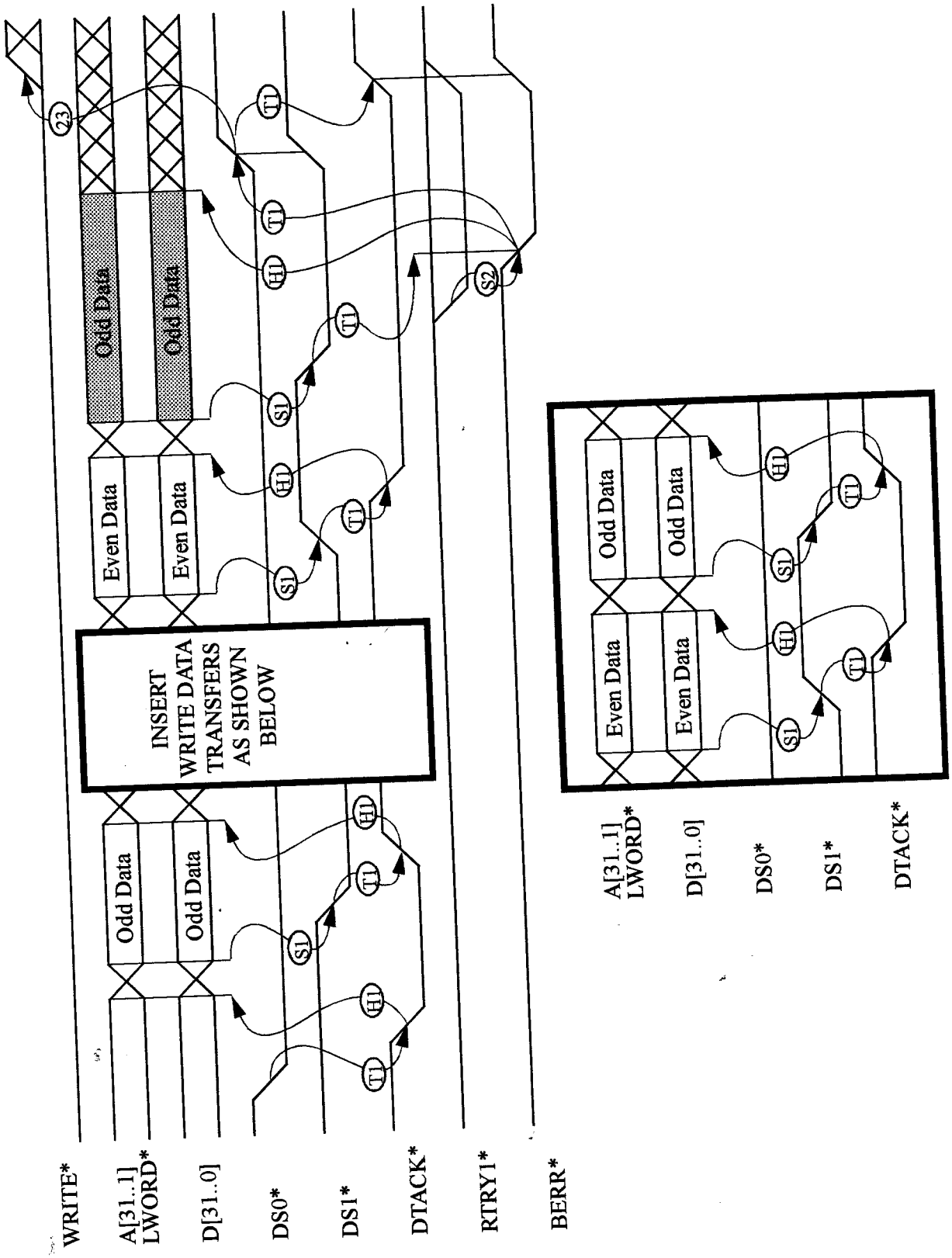

Figure 11-11 2eVME Write Data Transfers - Slave Terminated/Error on Odd Beat

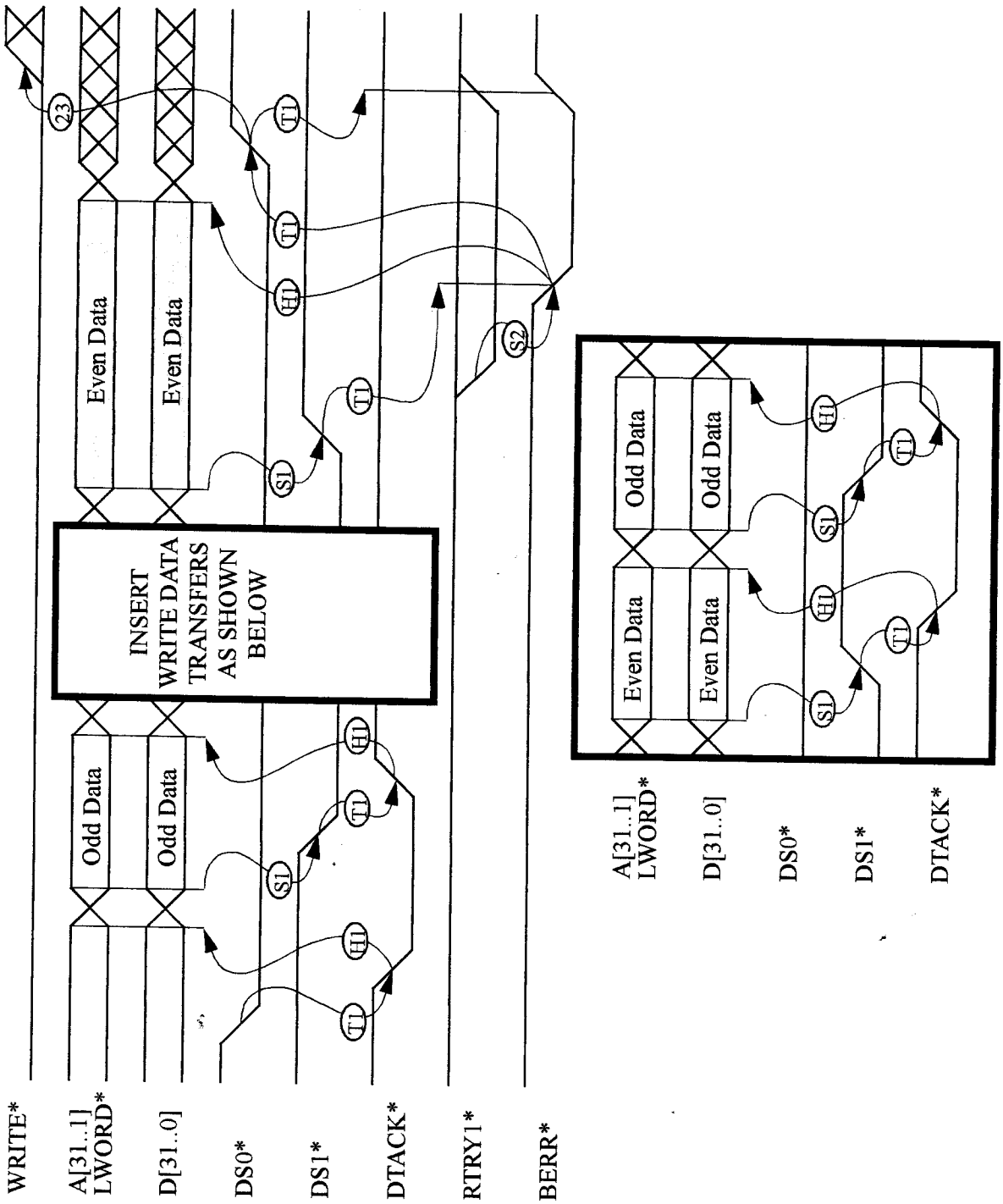

Figure 11-12 2eVME Write Data Transfers - Slave Terminated/Error on Even Beat