

Chapter 10

Additions to CR/CSR Definition

10.1 Introduction

A Configuration ROM / Control and Status Register (CR/CSR) Space is specified in Section 2.3.12 of the ANSI/VITA 1-1994, VME64 Standard. Standard resources within a VME module to support manufacturer and module identification, initialization, test and configuration are defined by twenty-four bytes in CR and three byte-wide registers in CSR. The use of the remaining 524,148 locations within the 512 KB CR/CSR space was not specified, nor was a method of allocating the space.

In this chapter, the utility of CR/CSR is enhanced in two ways. First, the definition of additional CR parameters and CSR functions makes more standardized information available to the system software, enabling automatic discovery of module and system components and automatic utilization of hardware capabilities. Second, the concept of Configuration RAM (CRAM) is introduced. Configuration RAM can be utilized by Value Added Resellers, System Integrators and End Users to store system configuration and initialization information. Storing such information within the module allows better fault isolation, which simplifies development of high-availability systems.

Following is a review of the characteristics of the VME64 CR/CSR Space as defined by the VME64 Standard.

- 1) Each module's CR/CSR Space is 512 KB in size (0x00000 to 0x7FFFF) and is part of an array of CR/CSR Spaces located in the region of VME64 memory decoded by the 0x2F AM code. A specific module's position in the CR/CSR Space array is determined by its CR/CSR Base Address Register (CR/CSR BAR). As originally written the method of loading the CR/CSR BAR was not specified, but it was implied that the Autoslot-ID mechanism would provide the CR/CSR BAR value. Chapter 3 of this document specifies that the CR/CSR BAR needs to be loaded based on the newly added geographical address capability.
- 2) The addresses within CR/CSR are specified as offset addresses. They are relative to the Base Address of the CR/CSR space. An absolute address in CR/CSR space is created by adding the offset address to the Base Address of CR/CSR space. Pointers specified in CR locations also contain offset addresses.
- 3) Each module's Defined Configuration ROM (CR) Area is located at the "bottom" (offset zero) of its CR/CSR Space. Addresses increase to the "top."
- 4) The CR area is "read-only" to the VMEbus regardless of the internal implementation. Information contained in the CR area should not be changed once a module is "on line" (i.e., ready to respond to bus data transfer cycles).
- 5) CR data can be one, two or four bytes in width. The spacing and access method to be used by VME64 masters when reading a specific module's User CR locations is determined by the module's CR Data Access Width parameter (see the VME64 Standard). The Defined CR Area (from 0x00 to 0x7F) is compatible with the D08(O) access method and utilizes only every fourth byte.
- 6) The Control & Status Register (CSR) area is located at the "top" of the CR/CSR Space.
- 7) The CSR locations can be modified after a module goes "on-line." Once a module is "on-line," its registers can be initialized or modified by itself or any VME64 master in the system.
- 8) CSR data can be one, two or four bytes in width. The spacing and access method to be used by VME64 masters when reading or writing a specific module's User CSR locations is determined by the module's CSR Data Access Width parameter (see the VME64 Standard). The CSR area offers read and write capability when accessed by VME64 masters.

- 9) The size of the implemented User CR and/or User CSR areas available on a VME64 module can vary by module (or even module revision) and can be zero.
- 10) Offset addresses and pointers are stored in big-endian order. That is, the most-significant byte of the object is stored at the lowest address and the least-significant byte is stored at the highest address.

A summary of the additional concepts and capabilities introduced in these extensions to CR/CSR follows.

- 1) Standard support for optional module-specific CR and CSR locations. This allows vendors the freedom to locate module-specific CRs and CSRs in suitable places (e.g. to ease address decoding) and set their sizes appropriately.
- 2) Standard support for an optional Configuration RAM (CRAM) area within CR/CSR space, including a mechanism to provide cooperating masters exclusive access to it.
- 3) Pointers in the Defined CR Area containing the beginning and ending addresses of a module serial number.
- 4) Characteristic parameters in the Defined CR Area allow identification of master capability, unaligned transfer capability, Read-Modify-Write (RMW) capability, Retry capability, presence of a P2 connector, presence of ETL transceivers, and Address-Only (ADO) cycle support.
- 5) Standardized support for programmable "Address Space Relocation". The purpose is to enable "plug-and-play" on VME by replacing DIP switches or jumpers with simple programmable address decoding. Parameters in the Defined CR area describe a module's address decoding capabilities. Registers in the Defined CSR area allow software to set base addresses for each of the possible address spaces within the module. A "Module Enable" bit is defined within the Bit Set / Bit Clear CSRs to allow use of the relocated address spaces once they have been initialized by software.

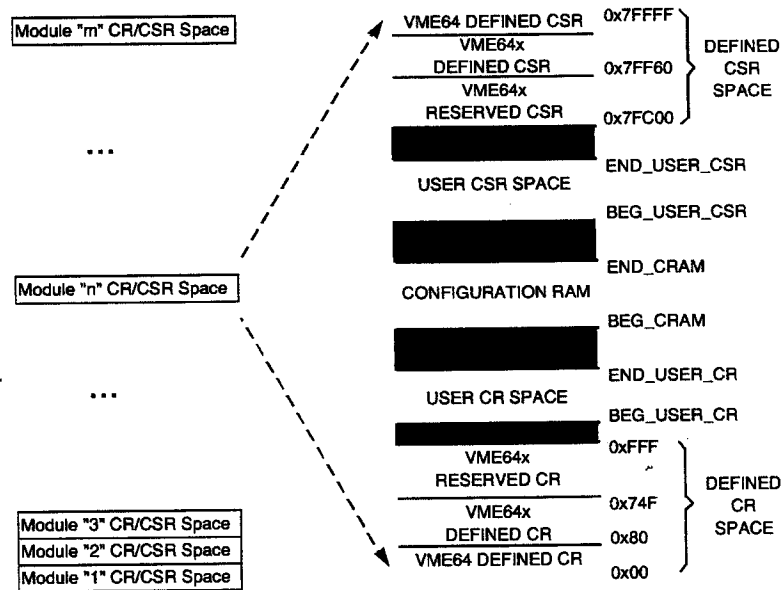


Figure 10-1: Structure of CR/CSR Space

Observation 10.1:

Although Figure 10-1 shows the User CR area below User Configuration RAM and the User CSR area above User Configuration RAM, the areas can be implemented in any sequence as long as they do not overlap.

10.2 Requirements**10.2.1 The Defined CR Area**

The Defined CR Area is composed of the locations at offset addresses 0x00 through 0x7F defined by the VME64 standard plus the additional Defined CR locations and reserved locations specified by this document, which end at offset address 0xFFF. Table 10-12 specifies the contents of these locations.

Rule 10.1:

The VME64x Defined CR Area shall be from offset addresses 0x000 to 0xFFFF (4KB). These locations shall only be used as specified in the VME64 Standard and as later specified in this document.

Rule 10.2:

All reserved or unimplemented locations in the Defined CR Area shall read as 0x00.

Permission 10.1:

Boards may use volatile memory (e.g., RAM) for the CR Area as long as it retains a "read-only" interface with the VMEbus.

10.2.1.1 CR/CSR Space Specification ID

In the VME64 Standard, the value contained at CR offset 0x1B specifies the revision of the CR/CSR definition. The definition as specified in VME64 is indicated by a value of 0x01. This specification is the second CR/CSR released version and is indicated by a value of 0x02.

Rule 10.3:

In the VME64x Defined CR area, address offset 0x1B shall contain a value of 0x02 when any of the additional CR/CSR features defined in this extension to the VME64 Standard are implemented on a VME64x module.

10.2.1.2 Module Characteristics Parameters

The Defined CR Area includes a Slave Characteristics Parameter and a Master Characteristics Parameter, whose formats are detailed in Tables 10-1 and 10-2. These allow modules to "advertise" their support for certain VMEbus features such as unaligned transfers and Read-Modify-Write (RMW). These are general capabilities. More specific capabilities are encoded in the AM and XAM Capabilities parameters outlined 10.2.1.4.

Table 10-1: Slave Characteristics Parameter

Bit	Value	Meaning
7	0	Slave does not support UnAligned Transfers (UAT)
	1	Slave supports UnAligned Transfers (UAT)
6	0	Slave does not support Read-Modify-Write (RMW)
	1	Slave supports Read-Modify-Write (RMW)
5	0	Slave does not support Address-Only (ADO) cycles
	1	Slave supports Address-Only (ADO) cycles
4	0	Slave does not support Address-Only with Handshake (ADOH) cycles
	1	Slave supports Address-Only with Handshake (ADOH) cycles
3	0	Slave does not support RETRY* and/or RESP*
	1	Slave supports RETRY* and/or RESP*
2	0	Slave does not implement P2 connector
	1	Slave implements P2 connector
1	0	Slave uses TTL transceivers
	1	Slave uses ETL transceivers
0	0	Reserved; always program this value
	1	Not to be used

Table 10-2: Master Characteristics Parameter

Bit	Value	Meaning
7	0	Master does not support UnAligned Transfers (UAT)
	1	Master supports UnAligned Transfers (UAT)
6	0	Master does not support Read-Modify-Write (RMW)
	1	Master supports Read-Modify-Write (RMW)
5	0	Master does not support Address-Only (ADO) cycles
	1	Master supports Address-Only (ADO) cycles
4	0	Master does not support Address-Only with Handshake (ADOH) cycles
	1	Master supports Address-Only with Handshake (ADOH) cycles
3	0	Master does not support RETRY* and/or RESP*
	1	Master supports RETRY* and/or RESP*
2	0	Master does not implement P2 connector
	1	Master implements P2 connector
1	0	Master uses TTL transceivers
	1	Master uses ETL transceivers
0	0	Reserved; always program this value
	1	Not to be used

Rule 10.4:

The Module Characteristics Parameters shall reside in the locations specified in Table 10-12 and follow the formats specified in Tables 10-1 and 10-2.

Permission 10.2:

Immediately following each Characteristics Parameter in the Defined CR Area is a User-defined Characteristics Byte. Vendors may use these bytes for additional module characteristics information.

10.2.1.3 Interrupt Capabilities

Two "Interrupt Capabilities" parameters are specified in the Defined CR Area. The Interrupt Handler Capabilities denotes which interrupt levels a handler can handle, while the Interrupter Capabilities denotes which levels an interrupter can assert. Both are bit-masks, so a bit programmed to "1" denotes support for the interrupt level corresponding to the bit's

position. For example, a value of 2 denotes support for interrupt level 1 only, while a value of 0xC denotes support for levels 2 and 3. Bits 7-1 are used for interrupt levels 7-1, and bit 0 is reserved.

Rule 10.5:

The Interrupt Capabilities Parameters shall reside in the locations specified in Table 10-12 and follow the bit-mask format given above.

10.2.1.4 Address Space Relocation

Geographically Addressed CR/CSR capability allows a module to be addressed upon system initialization and configuration without manually setting address switches. It avoids address conflicts and allows for modules to be moved around within a system and still be located and addressed without conflict. The addition of registers within the Defined CSR Area to provide software programmable Base Addresses for the functions within a module removes the requirement of providing hardware switch settings for Base Address assignment. System address maps can then be dynamically configured at system initialization by software programming. This is termed "Address Space Relocation". To avoid conflicts upon power up and during initialization, a module enable bit is provided in the Bit Set / Bit Clear register in the Defined CSR Area. Once the Function Base Address Registers have been programmed, the module can be enabled without conflict.

Support for Address Space Relocation is built on the assumption that a module can provide up to eight distinct "functions" which can be accessed using individual address decoders. Many modules provide only one function, but a specification must be flexible enough to accommodate the most complex cases (preferably without penalty for the simple cases). This specification allows a module designer to encode in CR, for up to eight functions, the data transfer sizes and AM and/or XAM codes it supports, and the bits its address decoder can compare (which implies the required allocation size). It must provide corresponding CSRs to allow programming of each function's base address. The specification also allows for a function's allocation size to be dynamic and provide multiple "access windows", without penalty for implementations not requiring these advanced features. Each function requires a set of CRs (DAWPR, AMCAP, XAMCAP, and ADEM) defined below, and one CSR (ADER) defined in 10.2.2.2.

Observation 10.2:

In some designs, the VME interface needs to be initialized and loaded with parameters, including the BAR. Clearly if the module was addressed before the interface was ready to respond, a BERR would occur. A good module design should ensure that if the VME interface is ready to respond, then all of the CR/CSR addresses are functional and contain valid information. A way to do this in a module design is to disable the VME interface until the module is initialized. If CR/CSR capability is implemented, it could be done starting the initialization with a BAR load of 0 (invalid) to ensure the interface is disabled, followed by module initialization, then interface initialization. The last step of the interface initialization would be to load the correct BAR and finally enable the interface.

10.2.1.4.1 Data Access Width ParameterS (DAWPRs) Definition

In the Defined CR Area, one Data Access Width Parameter (DAWPR) is assigned to each possible function. These parameters occupy one byte and specify the maximum data transfer bus width the function offers, as shown in Table 10-3.

Table 10-3: Data Access Width Parameter (DAWPR) Definitions

Value	Function
0x00	Feature not implemented
0x01 ... 0x80	Reserved
0x81	Accepts D08(O) cycles only
0x82	Accepts D08(E0) cycles only
0x83	Accepts D16 or D08(E0) cycles
0x84	Accepts D32, D16 or D08(E0) cycles
0x85	Accepts MD32, D16 or D08(E0) cycles
0x86 ... 0xFE	Reserved for future use
0xFF	Not to be used

Rule 10.6:

All implemented Data Access Width Parameters (DAWPRs) shall reside in the locations specified in Table 10-12 and adhere to the definitions in Table 10-3.

Recommendation 10.1:

The indications of support for UAT, RMW, ADOH and Retry are provided in the Slave Characteristics Parameter (Table 10-1). The fact that these are indicated in a single parameter rather than in each DAWPR implies that all functions should provide the same support for these features. This should not be a limitation, because these features are part of the data transfer logic rather than the address decoding.

10.2.1.4.2 AM Capabilities Parameters (AMCAPs)

There are 64 possible AM codes with values from 0x00 to 0x3F. The eight AM Capabilities Parameters (AMCAPs) in the Defined CR Area are 8 bytes wide, providing a 64-position bit-mask. Each bit, when set, indicates that the function can respond to the AM code associated with the position of the bit. For example, the AMCAP (0x00,00,00,01,00,00,08,00) indicates support for AM codes 32 (0x20) and 11 (0xB), because bits 32 and 11 are set. A master reading this parameter can determine all of the address spaces recognized by the function, as well as the block transfer and multiplexed block transfer capabilities of those functions.

Rule 10.7:

All implemented AMCAPs shall reside in the locations specified in Table 10-12 and follow the 64-position bit-mask, where each bit represents the respective implementation of an AM code.

Rule 10.8:

The AM code for CR/CSR Space (0x2F) shall not be set in any AMCAPs, because the corresponding address space relocation is realized by other mechanisms previously defined.

10.2.1.4.3 XAM Capabilities Parameters (XAMCAPs)

Extended Address Modifier Codes are described in Chapter 11 of this document. There are 256 possible extended AM codes with values from 0x00 to 0xFF. The eight XAM Capabilities Parameters (XAMCAPs) in the Defined CR Area are 32 bytes wide, providing a 256-position bit-mask. As with the AMCAPs, each set bit indicates that the function can respond to the Extended AM code associated with the position of the bit. For example, the XAMCAP (0x00,...,04) indicates support for XAM code 2, because bit 2 is set.

Rule 10.9:

All implemented XAMCAPs shall reside in the locations specified in Table 10-12 and follows the 256-position bit-mask, where each bit represents the respective implementation of an XAM code