any size conversion). Due to the fast clear feature of the 2249, however, this conversion time need be awaited only for valid events.

IMPORTANT: Care should be taken when using the 2249SG to ensure that all gates come within 2 μsec of the "Start" pulse. If this will not be true, the duration of the active clock may be increased by changing the 20K Ω resistor on IC "TD" (9602) to a larger value. Then the maximum allowable time between any two gates should be the new value of the monostable delay minus approximately 53.5 μsec.

2.10 Q and LAM Suppression

The 2249 Series was designed to permit one to eliminate the readout of empty modules if maximum readout rate is desired. An adjustable potentiometer (accessed from the side of the module) permits the user to define an "empty" module by setting a count level from 0 to 100 that must be exceeded before data is considered useful. A module in which all channels contain less than the set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. An X, Command Accepted, response is still generated.

Some branch drivers (interfaces between computer and CAMAC crate) require a Q response or a LAM from any module that occupies a station (N) in the CAMAC crate. For these situations, the L suppress feature may be defeated by removing the jumper XZ and replacing it with jumper YZ. (See schematic sheet 3 and Figure 2.2). In this situation the LAM is not suppressed and a LAM is obtained after any Read command. The Q-response suppress can be defeated by removing jumper VW and replacing it with jumper UW. To defeat both Q and L Suppress, it is only necessary to set the count level to 0. (NOTE: 2249's and older 2249A's do not have all the jumper options available on the P.C. board. These units will require the bus be cut and a jumper added on the solder side of the board).

2.11 Data and Readout

The output data of the 2249 Series is standard CAMAC compatible (TTL negative logic) in binary format. The 2249A and SG have 10 data bits plus an overflow bit. The 2249W has 11 databits and indicates an input greater than or equal to Full Scale by giving Full Scale (1980 counts) output. The digitized information plus overflow bit are gated onto the Dataway bus lines by F(0)·N·A, where F(0) signifies the read function, N signifies the 2249 to be read and A (from A(0) to A(11)) signifies which ADC channel in the 2249 is to be read out. Generally the unit is ready for readout when LAM appears. The function F(2) (Read and Clear) may also be used to read information from chosen ADC channels. However, this readout is destructive only when A(11) is addressed, the F(2)·N·A(11) clearing all channels at one time. The F2 command on addresses A(0) through A(10) will cause the ADC contents to be read with no clear and the input gate will remain disabled.

2.12 LAM

A LAM (Look-At-Me) signal is generated from end of conversion until a module Clear or Clear LAM (Z, C, F(2), F(9) or F(10)). LAM is disabled for

the duration of N, can be permanently enabled or disabled by the Enable F(26) or Disable F(24) function command, and can be tested by Test LAM F(8). LAM may be suppressed for empty modules as indicated in "Q and LAM Suppression" section above.

The test function F(8) allows the LAM to be tested. In response to application of F(8)•N•A (where A is from A(0) to A(11)) independent of Disable LAM, a Q response will be generated if LAM is set. Although the LAM is disabled while the 2249 in question is being addressed (i.e., for the duration of N), once latched it will produce a Q response when an F(8)•N•A is applied.

IMPORTANT: When current is applied to the 2249 (such as would occur when plugging a module in and turning the crate power supplies on), the states of the LAM latch and LAM enable are arbitrary. The unit must always be initialized with an F(24) (Disable LAM) or an F(26) (Enable LAM), and an F(10) (Clear LAM).

2.13 Packaging and Current Requirements

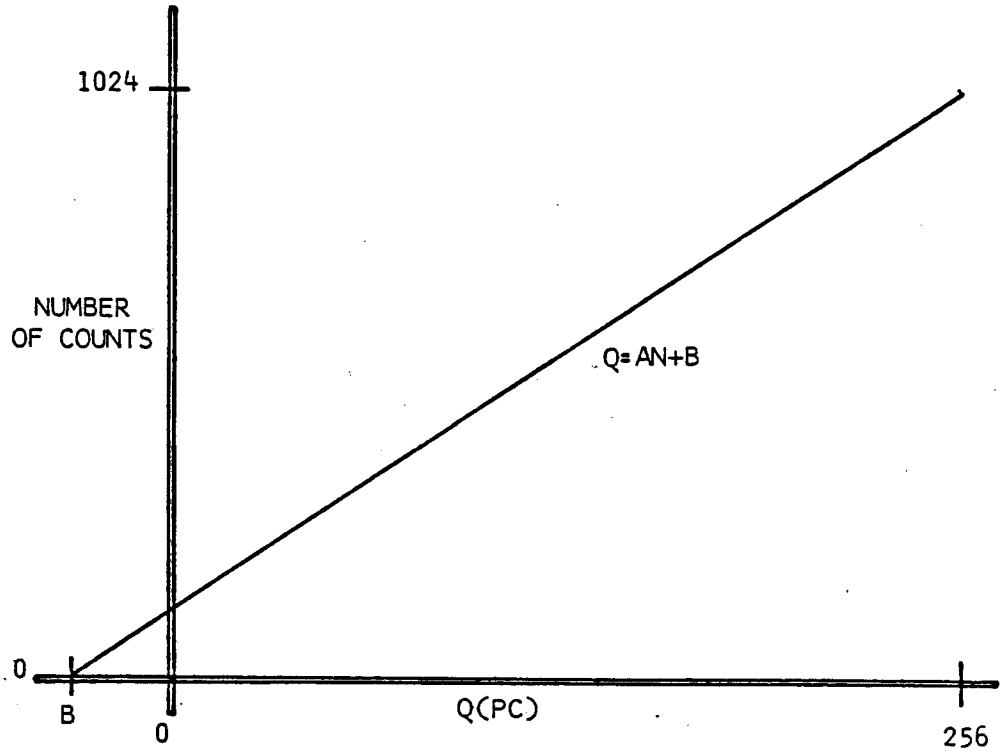
The 2249A and 2249W are packaged in a standard #1 width CAMAC module (conforming to ESONE Committee Report EUR4100). The 2249SG is #2 width. The A and SG versions dissipate a total of 7.5 watts and the W, 10.6 watts.

CAUTION: Because of the adjacency of the various voltage bus connector contacts in the CAMAC crate, plugging in any CAMAC unit may cause a momentary short of the power pins. This can cause severe damage to the module inserted, especially since the 24 volt pins are adjacent to the 6 volt pins. THUS, THE CRATE POWER SHOULD BE OFF WHEN A MODULE IS INSERTED OR REMOVED.

2.14 Inhibit Circuit

The standard 2249A and W have an automatic inhibit that prevents subsequent gate pulses from allowing more charge to enter the QTC after a first gate pulse is applied. This "self inhibiting" feature is not offered on the 2249SG. Therefore, caution must be taken to permit only one gate pulse per channel per event.

The Inhibit line of the 2249SG only affects the "Start" input, not the individual gates. Thus, gate pulses received during an inhibit period will cause charging of the integrating capacitor of the QT100C but no counts will be observed at the digital output. The gate pulse source should be externally inhibited whenever a CAMAC inhibit is applied. This function is easily performed if LeCroy Model 821 Quad Discriminator with Veto is chosen to drive the ADC gates.



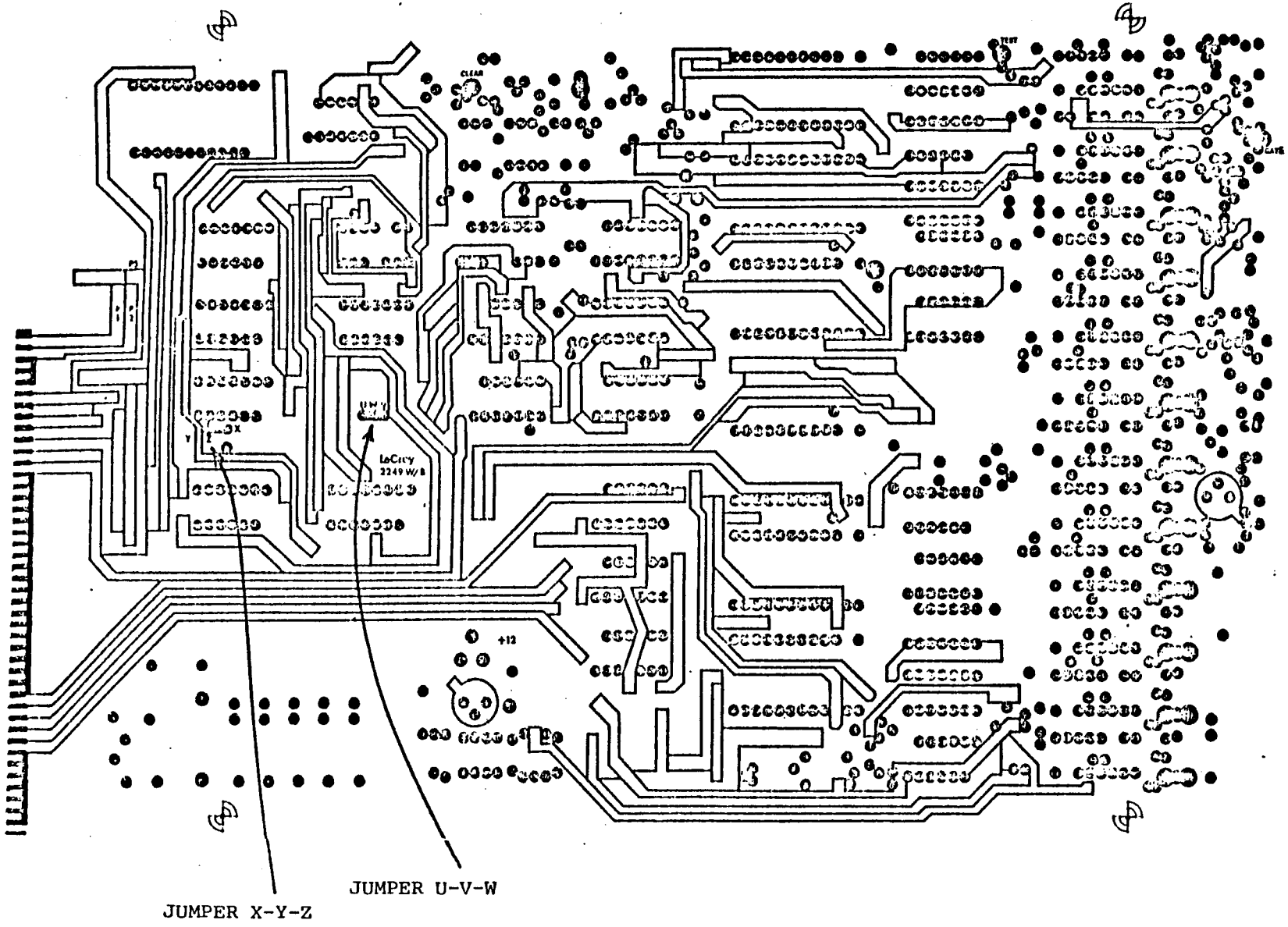
B IS AMOUNT OF PEDESTAL

Q IS CHARGE APPLIED TO ADC ANALOG INPUTS

N IS TOTAL NUMBER OF COUNTS

A IS CONVERSION SLOPE
I.E. A=(Q+B)/N

FIGURE 2.1



JUMPER LOCATION SIMILAR ON ALL 2249 SERIES UNITS

FIGURE 2.2

SECTION 3

TECHNICAL DESCRIPTION

3.1 General

The Model 2249 consists of 12 independent identical ADC's and associated circuitry. Referring to the 2249 Block Diagram in Figure 3.1, the 2249 circuitry is divided into 6 basic parts:

* Twelve QTC (charge-to-time converter) channels
* A gate, test, and pedestal circuit for distributing the gate signal to the separate linear gates of the QTC's
* Twelve clock synchronizers and scalers
* A controlled oscillator
* A Q response and L suppress circuit
* A CAMAC control section

Separate descriptions of each of these circuit blocks follow.

3.2 Charge-To-Time Converter

Each of the 12 inputs employs a hybrid change-to-time converter (QTC). A block diagram and waveforms for the QT100C are shown in Figure 3.2. The QTC consists of a virtual ground input amplifier, a linear gate driving a stable integrating capacitor, a current source, and an output differential amplifier.

The analog input of the 2249A and SG is a virtual ground with approximately 5 to 6 Ω impedance. It can be driven either from the front panel analog input via a 44 Ω resistor or from the common test input bus (which supplies each channel with an amount of charge proportional to the test input level supplied at the front panel or rear patch pin. (Without any TEST input, a high impedance connection to +12 volts generates an approximate 60% of full scale reading).

The QT100C and QT100B are identical and interchangeable. The letter change indicates only a change in method of manufacturing. These are used in the 2249A and SG. The QT102 is used in the 2249W and may not be interchanged with the QT100 series.

The front panel input has 44 Ω of resistance divided into two parts with input clamp diodes at their junctions to provide input protection and reduce crosstalk on large overloads. These resistors, in series with the low input resistance of the linear gate, terminate the input cable to 50 Ω. The stored charge is therefore $Q = \int_{T_g} (V_{in}/50\ \Omega)\, dt$ where V_{in} is the time dependent voltage on the analog input and T_g is the duration of the gate pulse. For the 2249A and 2249SG the current handling capability of the

input limits the linear range of the analog signal to -20 mA (or -1.0 volt across the 50 Ω input). On the 2249W the limit is -2.0 volts.

For the 2249A and 2249SG the required gate input signal is a standard NIM logic level, with recomended duration of 10 nsec minimum to 200 nsec maximum. The analog input is enabled for the duration of the gate.

The QT102 used in the 2249W employs a similar circuit, also with a 50 Ω input impedance. The input is, however, AC coupled via a 6.8 μF capacitor on the circuit board and minimum gate width is 30 nsec.

The charge delivered to the integrating capacitor through the linear gate is subsequently removed by means of a stable current source (see Figure 3.2). Thus, the voltage across the integrating capacitor is returned to its quiescent level at a constant rate. This rate is proportional to the difference between the +24 and V_{REF} inputs (Gain Adjust and +12 respectively, on block diagram). The output amplifier senses the voltage across this capacitor and generates an output level as long as this voltage is greater than a reference level (which is set by the 30 mV bias voltage). The output time duration (T) is therefore proportional to the input charge Q, where time T in microseconds is approximately 0.4 times the charge Q in picocoulombs (i.e., T = 0.4 Q μsec/pC). Operation of the QTC is assured by on-board stabilized ± 5 V supplies, keeping a perfect balance in the QTC. The V_{REF} (approximately +12 VDC) tracks the +24 VDC supply, causing the difference (used as the current source reference) to be independent of external supply variations. A small fixed amount of charge is always put into the analog input when a gate pulse is generated. The pedestal of each ADC channel has been factory calibrated to be equivalent to a few picocoulombs input (for gate pulse widths of 50 nsec) when all the inputs are externally loaded with 50 Ω terminations. If the inputs are not terminated, a slightly lower reading will be observed.

A Clear command can be used if desired to clear the 2249 during a conversion cycle. It not only initializes all the digital control and scaler stages, but also, via a leading edge R-C differentiator, clears the analog ramp of the QTC to its quiescent level. The analog clear pulse width is about 300 nsec, leaving the remainder of the digital clear time for settling in the QTC.

3.3 Gate, Test and Pedestal Circuit

The gate generator is operated by either a front panel NIM input signal or by an increment signal supplied by the CAMAC controller. The internal gate pulse will actually enable the analog inputs of the A and SG versions about 4 nsec after application and the W version, 7 nsec after. It should, therefore, precede any input by at least that amount. The actual duration will be equal to the input plus about 4 nsec for the A and SG versions, 5 nsec for the W. The increment pulse supplied by the CAMAC control section generates an approximately 80 nsec wide gate pulse (see schematic, sheet 3, and Figure 3.3 upon application of an F(25). Its action is to enable the gate and generate a test pulse.

The test input of the 2249A and W is connected through a precision resistor to a common capacitor in the test circuit. The charge which is stored in

this capacitor is equally shared by all channels. The CAMAC Inhibit must be used when testing the unit with F(25). On an INRC command, F(25)·S2, the CAMAC control generates a pulse which is OR'd into the gate circuit. In addition, if an inhibit condition exists, INCR discharges the test capacitor equally into the 12 QTC's during the gating interval. The test input accepts a positive DC level of 0 to 20 volts to produce a zero to approximately full scale digital output of each ADC.

The trailing edge of the output of the gate generator also produces an initiate pulse which is used to set the busy latch and generates the delayed pulse which starts the conversion cycle. The busy latch feeds back to inhibit the gate within 100 nsec of the trailing edge and is cleared by the reset pulse.

The pedestal is adjusted by injecting charge via a trimmer capacitor (C_{PED}) into the virtual ground of the QTC from the leading edge of the gate pulse where the amount of charge is proportional to the C_{PED} in pFd times the voltage swing of the gate pulse. The trailing edge of the gate is not coupled in because the gate closes and blocks the charge. Because of the charge injection time constant, gate widths narrower than 50 nsec (500 nsec) will not allow all of the injected pedestal charge to be accumulated by the 2249A (2249W). This causes a reduction of the pedestal reading somewhat faster than indicated by the gate dependent term in the specifications.

3.4 Clock Synchronizer and Scaler

The output of each QTC hybrid in the 2249 Series is used to gate an oscillator into one half of a LeCroy hybrid SC100 Dual Eleven-Bit Scaler. The oscillator is synchronously started with respect to the leading edge of the gate (see section 3.5). This ensures no fractional pulses during the beginning of the rundown cycle, but care must be taken at the end of the rundown. This is done by the synchronizing stage. Each gate circuit (see schematic sheet 2, and Figure 3.4) supplies an integral number of clock pulses even if the QTC output returns to its quiescent state in the middle of a clock pulse as shown in the figure.

When the conversion cycle is complete, readout of the addressed scaler can be done by enabling the proper SC100 (using decoded A2, A4, and A8 subaddress lines) and selecting the proper half of the SC100 (using the A1 subaddress). The data will be gated out in parallel to the CAMAC dataway.

3.5 Controlled Oscillator

The clock circuit is a modified Colpitts oscillator employing a highly temperature stable choke and a mica capacitor as its resonant elements. Its frequency is 20 MHz. The oscillator is gated on 2.2 μsec after the leading edge of the gate pulse. Gating the oscillator in this way eliminates the uncertainty of one count associated with an asynchronous oscillator and eliminates noise and nonlinearities caused by not delaying the turn-on (see Figure 3.5). The conversion time is set to 60 or 105 μsec allowing more than enough time for the nominal 50 μsec or 100 μsec full scale conversion to occur for the 2249A and SG or W, respectively. This allows for the ±5% differences from channel to channel, slight temperature drifts, module to module variations, etc., and still ensuring that an overflow can occur for

oversized input pulses.

3.6 LAM and Q-Response Suppress Circuit

At the beginning of the gate pulse, a monostable is set (see Figure 3.5). The RC time constant of this monostable is adjustable by a side panel potentiometer labeled Q and L SUPPRESS LEVEL ADJUST. When the monostable resets, a latch is reset if one or more of the QTC outputs is still on. If set, this latch disables the Q-response circuit (that normally indicates valid data on an F(0) or F(2) Read Command) and clears the LAM. Disabling of the suppress function can be done for either Q-response or L. See Operating section 2.10 for more information.

3.7 The CAMAC Control

The decoding of CAMAC "F" functions and N is performed by a 4 line to 16 line decoder (an SN74154). A DC level is generated at the appropriate pin for each valid CAMAC command. Scaler addressing is accomplished using a 4 line to 10 line decoder (an SN7442) on A2, A4, and A8, to enable the appropriate SC100 scaler hybrid and the A1 bit is used to select the appropriate half of the SC100. X-response is generated for all valid commands, and Q-response and LAM are generated as described in the Q and L Suppress Circuit section.

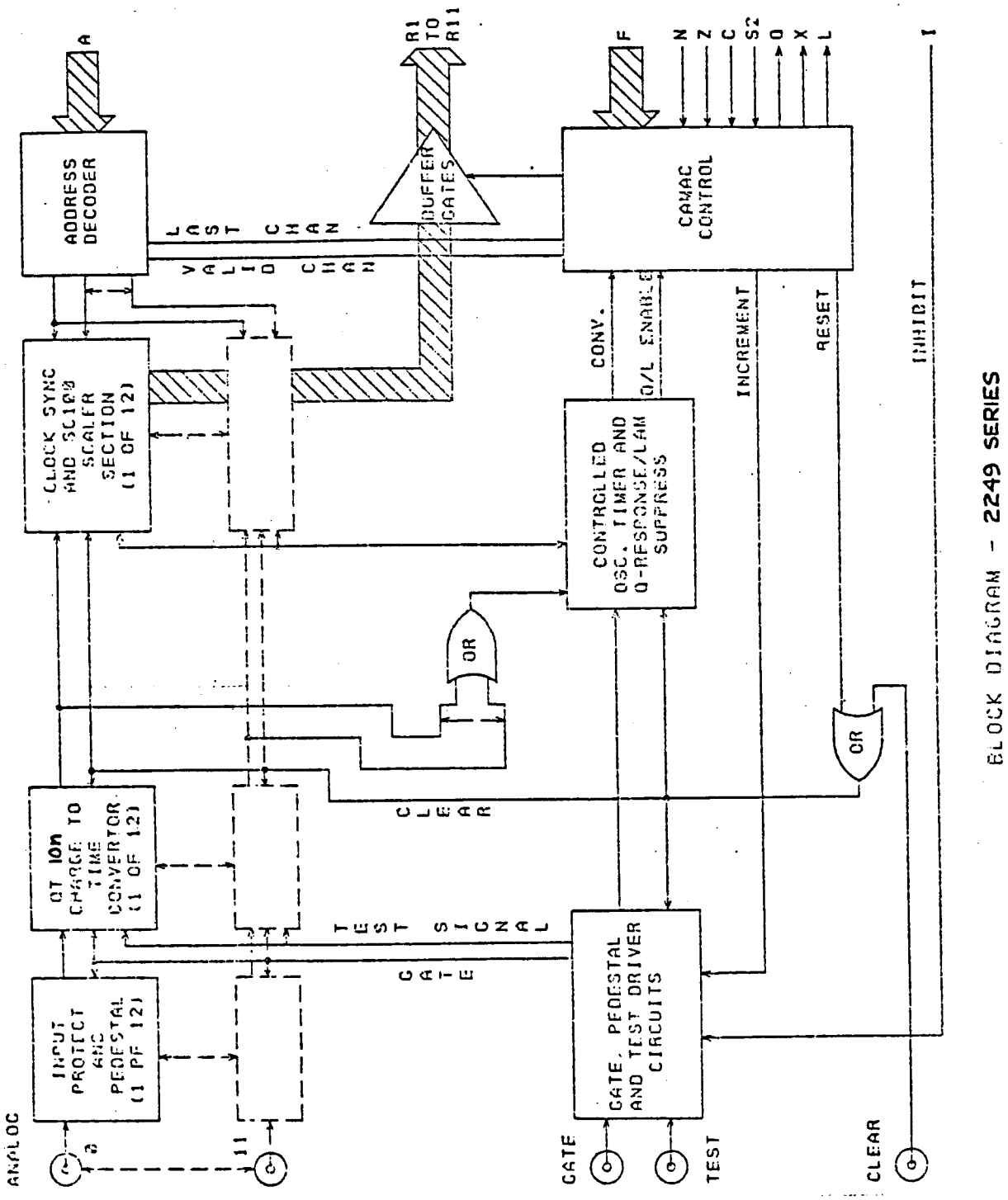
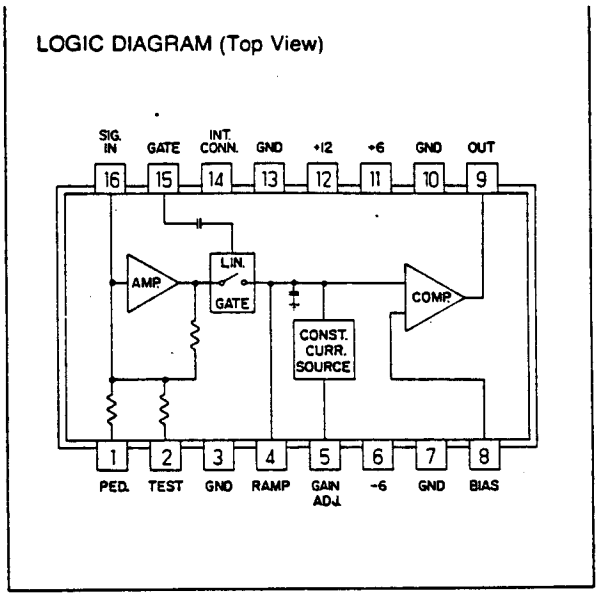
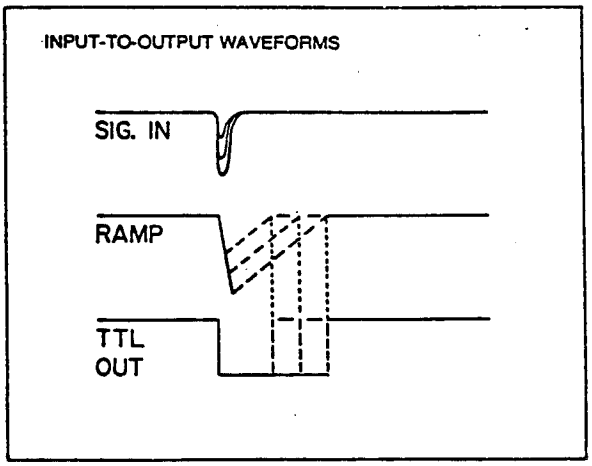

BLOCK DIAGRAM - 2249 SERIES
ADDRESS DECODER
A
R1 TO R11
BUFFER GATES
LAST CHAN
VALID CHAN
F
N
Z
C
S2
Q
X
L
CAMAC CONTROL
CLOCK SYNC AND SCALER SECTION (1 OF 12)
CONV.
G/L ENABLE
INCREMENT
RESET
INHIBIT
CONTROLLED OSC. TIMER AND Q-RESPONSE/LAM SUPPRESS
OR
OR
CLEAR
QT ION CHARGE TO TIME CONVERTOR (1 OF 12)
TEST SIGNAL
GATE
INPUT PROTECT AND PEDESTAL (1 OF 12)
GATE, PEDESTAL AND TEST DRIVER CIRCUITS
ANALOG
2
11
GATE
TEST
CLEAR

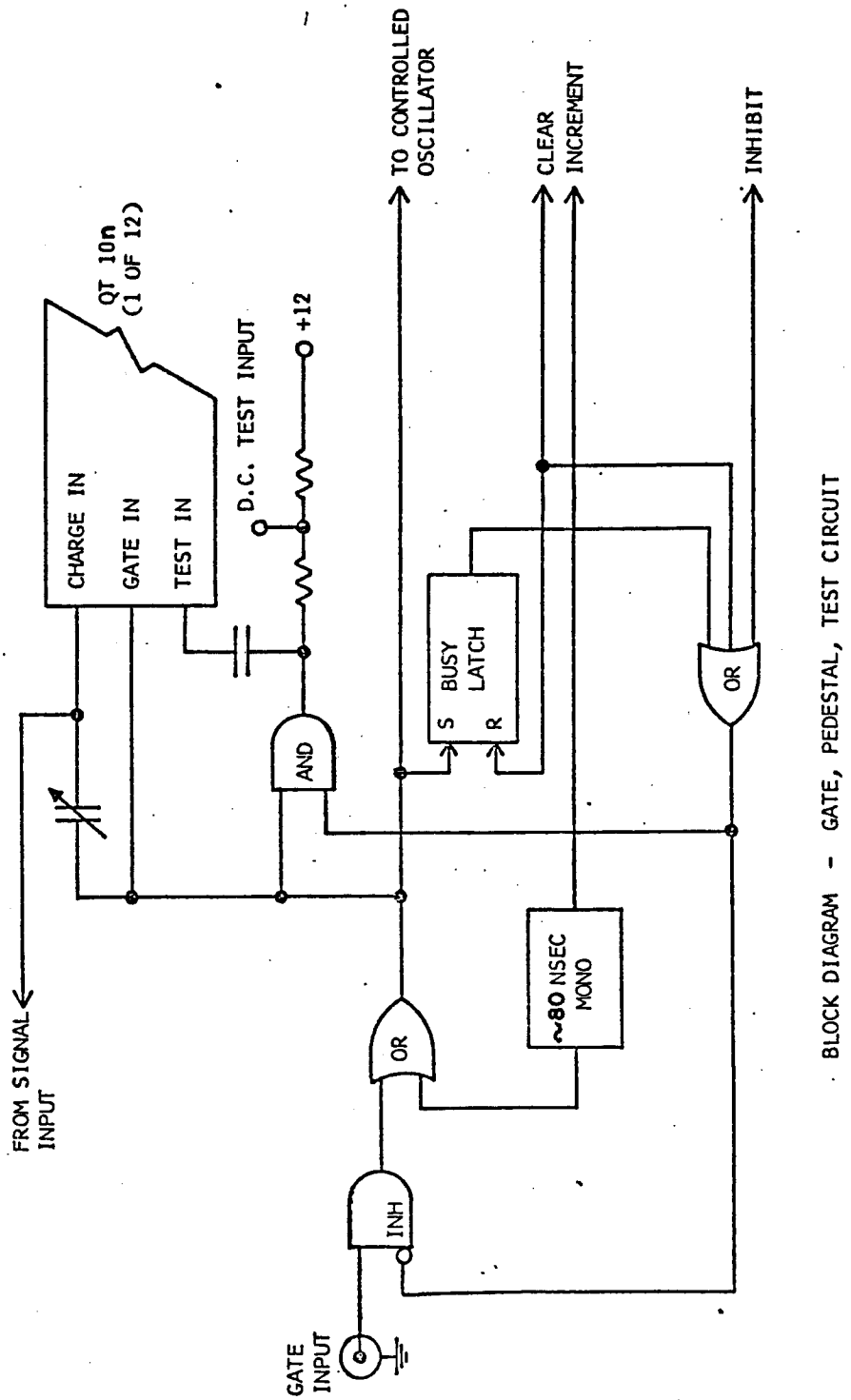
FIGURE 3.1





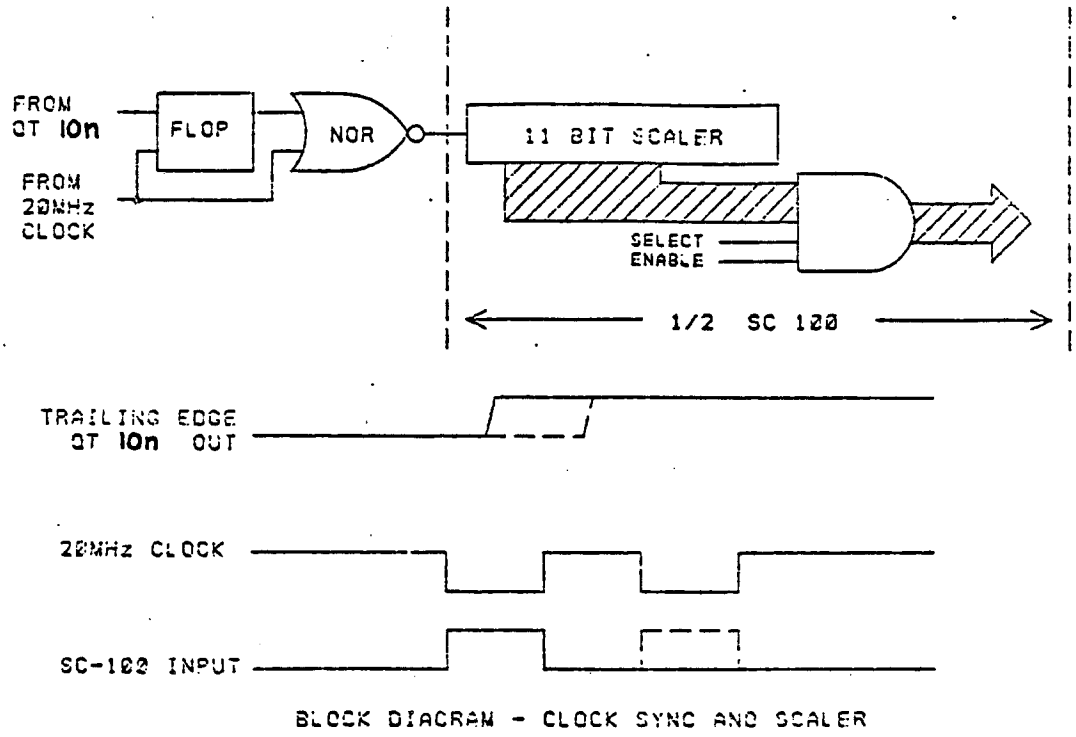
QT100C

FIGURE 3.2



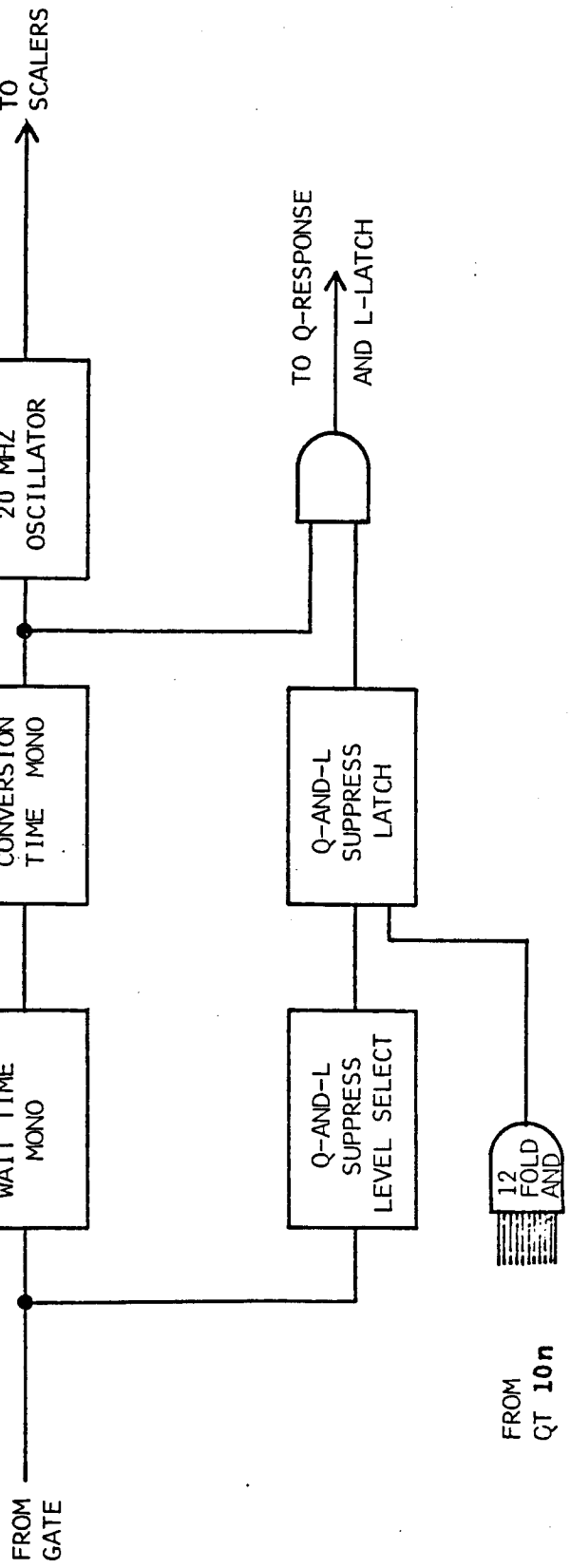
BLOCK DIAGRAM - GATE, PEDESTAL, TEST CIRCUIT

FIGURE 3.3



BLOCK DIAGRAM - CLOCK SYNC AND SCALER

FIGURE 3.4



BLOCK DIAGRAM - CONTROLLED OSCILLATOR AND Q-RESPONSE AND L SUPPRESS

FIGURE 3.5