Klystron Modulator Microcomputer Control Units

Roger Bissonnette

Photon Factory, KEK

Abstract: Design philosophy, equipment configuration and functions, present status and major difficulties of the Photon Factory Injector klystron modulator control system are described.

Introduction

The 2.5 GeV injector linac for the Photon Factory storage ring gets its rf power from 42 S-band klystrons, each capable of 30 MW pulse output, remote control is essential for successful operation. Further because the expense of dedicated control wires continues to go up while the cost of general purpose microprocessors has become so small it was natural to plan a microprocessor based controller for each klystron modulator.

From the control point of view each modulator is very simple conceptually. A collection of status points is interlocked to control the sequencing of the various internal power supplies etc. Once the klystron has come on-line there are really only two parameters which directly affect the acceleration of the electron bunches: the low-level input rf phase and the klystron anode potential.

The power available for acceleration depends on the anode potential of the klystron, and any small variations cause deleterious phase modulation of the output. Therefore in this case the voltage to which the Pulse Forming Network is resonantly charged must be closely controlled, and as is usually done a De-Q'ing circuit is introduced for that purpose. The now stable rf phase may be set by a phase shifter in series with the klystron input. Because of the importance of these two functions there are two identifiable boxes that implement them; the De-Q'ing trigger controller and the IϕA unit.

The necessary status interlocking and sequencing mentioned above have been pulled together and put under local control in a unit called Control-I. This hardware controller, designed by S. Anami and his team in the rf source group, along with isolated operation of De-Q and IϕA allows complete stand alone test and operation of any modulator. Thus a modulator can be operated safely without need for the remaining remote control functions.

The remaining functions; parallel monitoring of modulator status, sequencing, communications between the central control network and with De-Q and IϕA are assigned to the last of the 3 units to be discussed here, Control-II.

De-Q

A Motorola 6802 type microprocessor (MPU) with a 6850 ACIA serial interface and a 12 bit DAC execute firmware residing in a small portion of a 2716 type 2 k EPROM. The serial data and DAC are optically isolated from the MPU. Making this a separate unit allows keeping the critical DAC output setpoint voltage signal line short and this reduces noise problems. Remote commands etc. are communicated at a 48 kbps rate asynchronously using the 6850 ACIA.

The De-Q and IϕA are in a serial loop with Control-II as the master station.

IϕA

This unit is also based on a 6802 MPU, 6850 ACIA and 2716 EPROM along with the addition of a stepping motor to rotate the phase shift unit, and an incremental rotary encoder to allow reading back the nominal electrical phase to within ϕ.5°. The first 15 units were built with a 8:1 gear reduction between the stepping motor and the phase shifter. Each motor step then is ϕ.45°, which is too large a step and since the amount of inertia and friction damping is very small the servo loop dynamics are quite bad.

Control-II

This unit is the only one dedicated to a remote control function. It is housed in a CAMAC-like crate with its hardware partitioned into 8 modules: a master CPU module for executing the main program and also interfacing a serial loop to De-Q and IϕA, 5 modules are involved with interfacing to Control-I, a link interface module manages the klystron modulator node on a 500 kbps loop network and a maintenance module inserted on an as-needed basis provides access to the CPU bus. Three MPU's provide distributed computing power: besides the master MPU there is a MPU in the status interface module. Using its input interface to Control-I and an associated LED display module the MPU firmware can capture which status conditions first changed. The link module also has a MPU for implementing a HDLC like protocol. Since there are 8 klystron modulators/loop there is much traffic on this high speed link. The module exchanges completed messages addressed to the particular klystron modulator with the main CPU. The remaining modules in the Control-I interface group are a control module with 12 relay contacts which provide parallel functions for the local push buttons sequencing the modulator on and off and a pair of modules for a floating optically isolated 12 bit successive approximation ADC. The ADC has a 32 channel input multiplexer. On each acceleration trigger many critical pulse peak values etc. are acquired by Sample/Hold buffers for conversion during the minimum 20 ms before the next bunch is accelerated.

Present Status

First prototypes of all the modules and boards have been tested piecemeal under noise-free conditions to verify that all the basic required functions are in fact working. 15 IϕA controllers have been built. The De-Q'ing controller design will be released for production this month and planning for a second prototyping of Control-II before quantity production is proceeding apace. Main problems encountered to date have involved noise margin, stability and program development and testing.

Noise Strategy

All of the hardware described is physically mounted in the klystron modulator, albeit in the rack furthest from the klystron. This puts it in an extreme electromagnetic noise environment. Accordingly what we are trying to do is to use ordinary TTL, Low power Shottky TTL and NMOS LSI and then to gain sufficient noise margin by careful design and attention to grounding and shielding. RF noise filters are put on the inputs of all power supplies, opto-isolators break the flow of current loops on inputs and outputs. PCB power distribution in Control-II is made with Vcc/Gnd bus bars to present lower impedance, and generous use of decoupling capacitors is made. Optical fiber is used for the 500kbps loop which covers some meters in the klystron gallery. The 48kbps lines are short, 40 mA push-pull current loops received

by opto-isolators.

In the hopefully rare but not impossible event that a MPU program does get hung in an "infinite loop" there are watch dog timers which if not strobed periodically by instructions in the main loop automatically reset the processor.

Stability

The analog subsystem must be long-term stable to at least better than 0.2%, with even better short term stability. The de-Q'ing controller DAC looks like it will be OK, but the first ADC module was not acceptable. A Burr Brown hybrid linear opto-isolator (3650 kG) was used which had marginal linearity and bad temperature drifts. The next ADC will try putting the isolation in the digital output of the AD which should improve performance and reduce price considerably.

Program Development and Testing

Aside from the direct expenses in procuring and otherwise assembling and testing the system, there is a large continuing effort involved in this sort of special purpose hardware and software development. Beginning about 18 months ago with a basic Hitachi SD-10 paper tape system and a Tektronics universal logic analyzer the development system has been upgraded to include the rather formidable array in Table 1.

Programs are being written in relocatable assembly language routines, and thus code which can be used in common by different processors can be simply link edited together to make the programs for the various processors. This also facilitates assembling and debugging smaller routines in a more systematic manner.

In terms of program complexity the biggest problems so far have been coding the communications (master-slave sides), error recovery and the IϕA stepping motor-rotary encoder.

Programming the loop handlers is complicated by the speed of transmission, 36 machine cycles/character at 500kbps and 229 at 48kbps, and also by the large number of states the two finite state machines can get into.

The IϕA program turned out to be harder than expected most likely because of the tendancy to have overshoot oscillation in the vicinity of a rotary encoder transition point but possibly because of noise pickup; sometimes the input from the rotary encoder shows an "impossible transition in which case knowledge of the exact phase angle is lost.

Finally, while costs may often only be of tangential concern in a scientific project, the economics are absolutely crucial for this kind of engineering development work. For this reason the approximate costs of the development system and prototype hardware are included in Table 1.

Acknowledgements

The overall system design, loop network architecture and much of the detailed design must be credited to K. Nakahara of the Photon Factory who has almost single handedly done most of the work. The Control-II design was completed and debugged by M. Matsuno of Kuwano Electric. The De-Q and IϕA boards were layed out and assembled by Kaizu Seisakujo of Kodaira.

Table 1

Major Software Development System Components

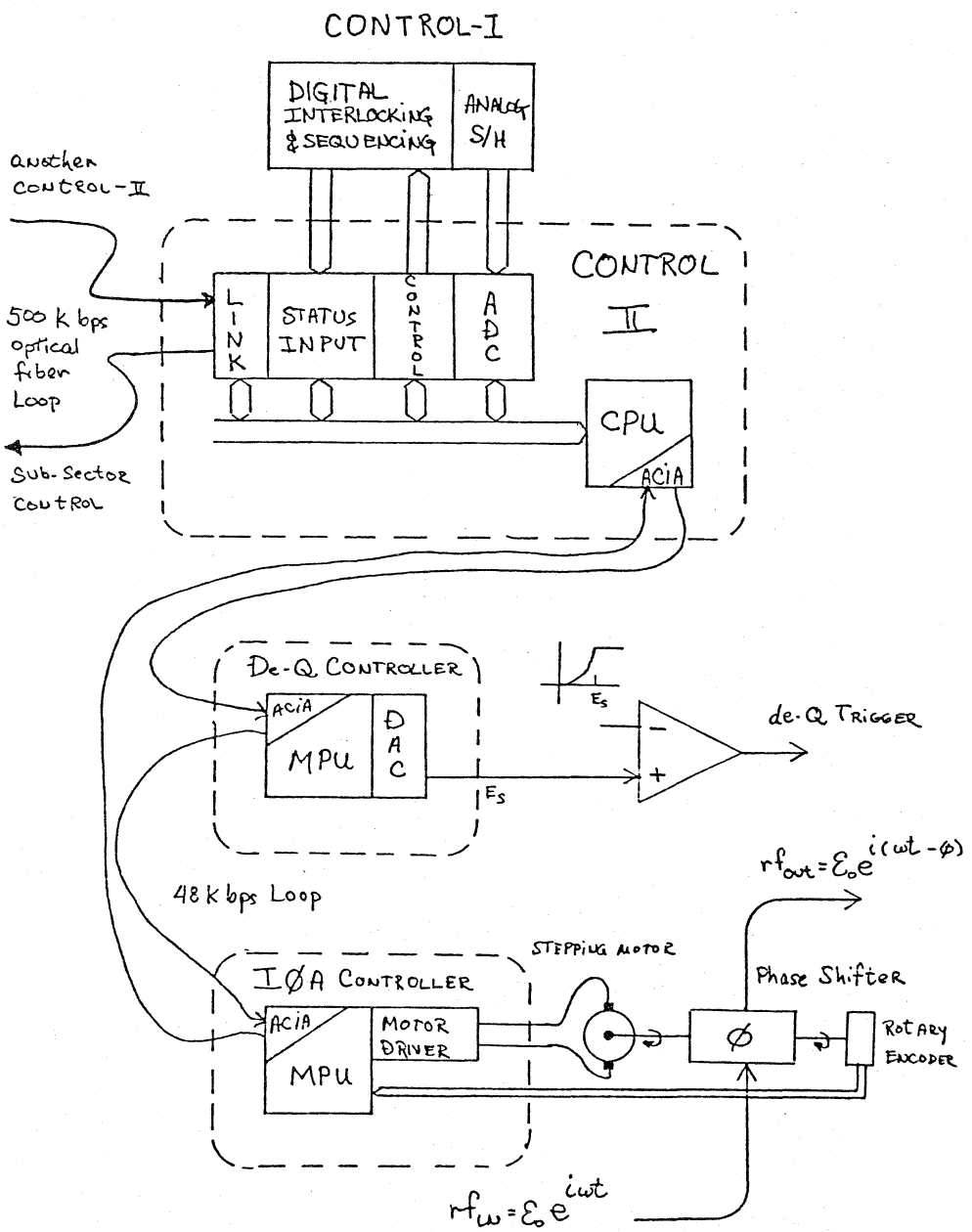
Hitachi H68/SD-10 Microcomputer Development System	¥ 910,000
H68/T402D Dual Floppy Disc Drive & FDOS-II Operating System	¥ 1,491,000
H6S/PW02 PROM Writer	¥ 170,000
Sharp IO 0263 Sharpwriter	¥ 819,000
General KDE-810 Character Display	

Hardware/Software Debugging Tools

Takeda Riken TR-4720 Logic Analyzer & 6800 Personality kit	¥ 1,590,000
Hp 5004A Signature Analyzer	¥ 270,000

Hardware Prototype Direct Costs

Control-II	
De-Q Controller board	¥ 150,000
IϕA Controller board	¥ 100,000



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