STABILIZATION OF ACCELERATING FIELD USING FPGA FOR J-PARC LINAC

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Abstract

The FPGA based digital RF feedback (FB) system installed in a compact PCI (cPCI) is applied to the J-PARC linac in order to realize the accelerating field stability of ±1% in amplitude and ±1 degree in phase [1]. The FPGA board with software developed using Xilinx ISE performs the real time feedback calculation of the accelerating field [2]. A DSP board is used for digital signal processing and monitoring, cavity tuner controlling, and communication between FPGA and CPU. The FPGA feedback control system will be explained in detail in this paper. The feedback and cavity tuner control tests with the newly improved software have been performed by using DTL2 cavities and waveguides in June and July 2006, and the required stability of the accelerating filed has been successfully achieved.

INTRODUCTION

The feedback control system is shown in Fig. 1. A PLC is used as the main controller for RF and FB ON/OFF and parameter setting [3]. The digital feedback system is installed in the compact PCI (cPCI), which consists of CPU, IO, DSP with FPGA, Mixer & IQ modulator, and RF & CLK boards [4]. The RF & CLK board receives the distributed reference optical signal (312MHz) from the master oscillator, and generates synchronized RF (324MHz) and clock (12MHz and 48MHz) signals.

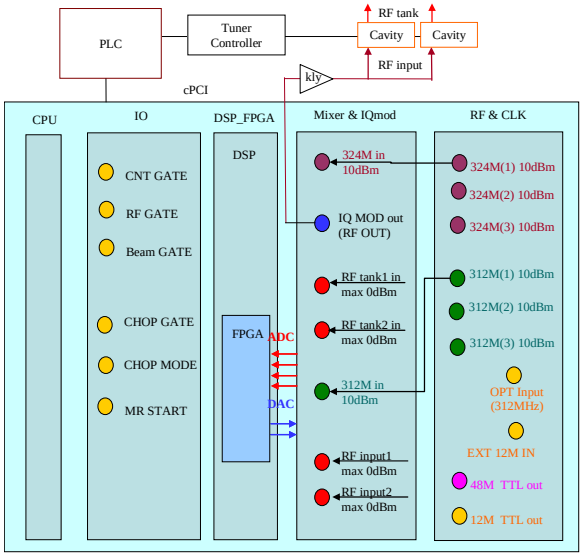

Figure 1: Feedback control system with PLC and cPCI.

The block diagram of the feedback system is shown in Fig. 2. The 324MHz RF drive signal delivered from the RF & CLK board is modulated through the IQ modulator and transmitted to the cavities after amplified by a 324MHz klystron. Each klystron drives two cavities. The RF signals of two inputs (RF input, 324MHz) and two outputs (RF tank, 324MHz) are down-converted to 12MHz signals by mixers, and these 12MHz mixer output signals are directly connected to the 14-bit ADCs in the FPGA board. The real time feedback processing is performed at the FPGA board, which is explained in the next section. The DSP board is used for digital signal processing and monitoring, cavity tuner controlling, and communication between FPGA and CPU.

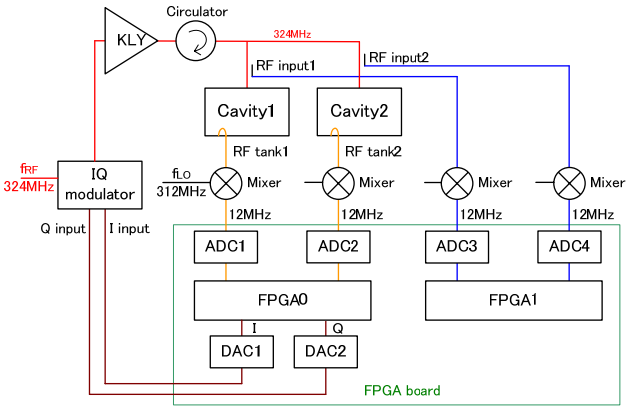

Figure 2: Block diagram of feedback system.

FPGA FEEDBACK CONTROL

The FPGA board consists of two FPGAs (Xilinx XC2V2000) as shown in Fig. 2. The FPGA0 is used for real time feedback processing of the accelerating field. The FPGA1 is used just for measuring I and Q components of the RF input signals to the cavities, and the data are sent to the DSP for cavity tuner controlling.

The feedback control diagram of FPGA0 is shown in Fig. 3. In the left side of Fig. 3, the three input gate signals, CNT_GATE, RF_GATE, and BEAM_GATE, come from the J-PARC timing system via the IO board. The RF and FB ON/OFF are operated though a PLC touch panel.

At first, the 12MHz down converted ADC signals of accelerating fields (RF tank) are sampled at 48MHz clock and transferred to I and Q components. Then, the calculation of IQ conversion with amplitude calibration and phase rotation are carried out.

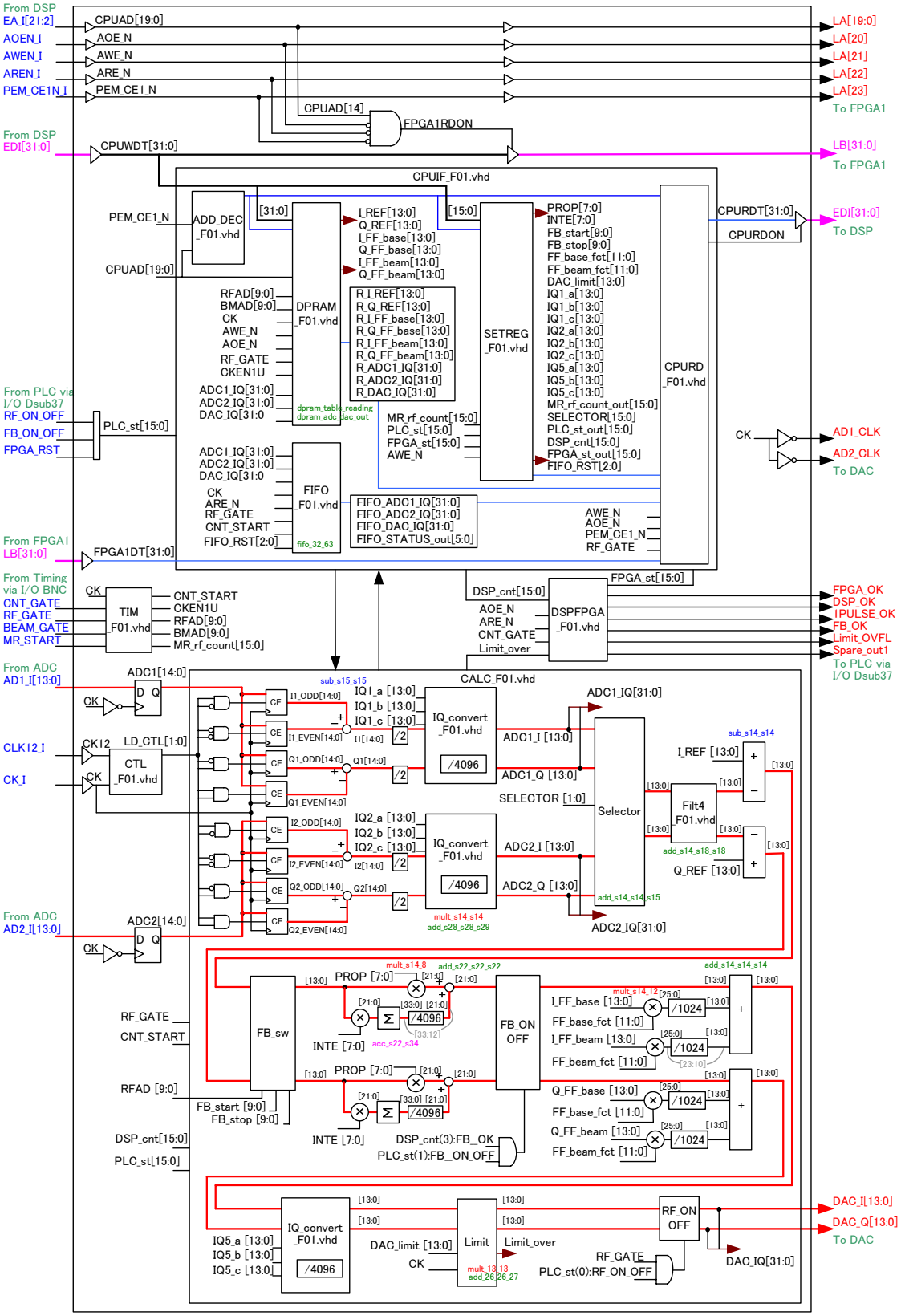

Figure 3: Feedback control diagram of FPGA0.

The calibration parameters of amplitude factor and loop phase for each cavity should be determined in advance by measuring the cavity output signal (RF tank) when a required power is fed to cavity with FB OFF.

Figure 4 shows the feedback control block of the FPGA0. The selector is used to choose which one of the cavity field will be applied in the feedback calculation loop, cavity 1 or 2, or average field of them. It is convenient for checking program. For the usual operation in the future, the selector for average field of cavities will be adopted.

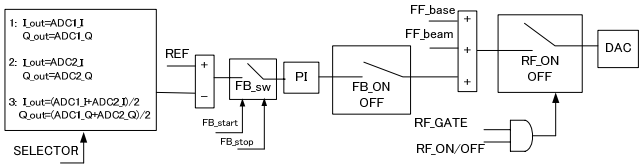

Figure 4: Feedback control block of FPGA0.

The reference table (REF) is used for feedback setting. The general FB ON/OFF is controlled by the PLC and DSP. Besides, a feedback switch in the waveform is designed, which is turned on between the start and stop times, for example, during the flat top of RF pulse.

A PI controller is used in the feedback loop. Two parameters, PROP and INTE, are also controlled through the PLC touch panel.

The two feedforward tables, FF_base and FF_beam, are provided for compensation of accelerating field and beam loading respectively. The timings of the two tables are independent, referring to RF_GATE and BEAM_GATE respectively. Thus we could adjust the start time of the beam compensation accurately with a time step of 48MHz clock, and get a flat top of RF pulse of the accelerating field even with the beam loading.

The general RF ON/OFF is controlled by both the PLC and RF_GATE. After confirming not over the limit setting, the FPGA outputs of I and Q will be sent to the two 14-bit DACs if RF ON/OFF is ON. Then the DAC outputs are connected to the IQ modulator as shown in Fig. 2.

All of the control parameters are set in the DSP through the PLC touch panel. In the FPGA, after decoding the address of those DSP data, the setting tables (REF, FF_base and FF_beam) will be processed in the DPRAM block, and the other control parameters will be read out through the SETREG block, as shown in Fig. 3. Then these control parameters will be used in the calculation of FPGA signal processing.

The I and Q components of RF input and RF tank signals (ADC1_IQ, ADC2_IQ, ADC3_IQ, and ADC4_IQ) and the I and Q data of FPGA outputs to DACs (DAC_IQ) will be sent back to the DSP through the CPURD block. Thus, the DSP will monitor the status of FPGA in real time, including the waveform of accelerating field.

During the signal processing in the FPGA, the I and Q components of RF tank signals (ADC1_IQ and ADC2_IQ) and the I and Q data of FPGA outputs to DACs (DAC_IQ) will be saved in the FPGA FIFO with 4MHz clock. The FIFO data will be sent to the DSP. Then the DSP will process those data to check the waveform of RF signals, and control the feedback system in real time.

FEEDBACK AND CAVITY TUNER CONTROL TESTS

In the last year, the test of stability of the accelerating field using this FPGA based digital RF feedback system had been carried out, and the test results had been reported in the reference paper [4]. The stability of ±0.2% in amplitude and ±0.2 degree in phase had been successfully achieved.

In June and July of this year, the feedback and cavity tuner control tests using the newly improved software, which is described in the above section, have been performed by using DTL2 cavities and waveguides. The DTL2 cavities have two input ports. In our test, one port is used as normal input port, and the other port is used as pickup port of the cavity voltage. The test results show that the same stability of amplitude and phase of the accelerating field as before have been successfully achieved again. Furthermore, if we move the tuner position designedly to make phase shifting up to about 45 degrees, the auto cavity tuner control will start to drive the motor to move the tuner back to near the original position to make the phase shift less than 0.2 degree, and it takes only about 10 seconds for phase controlling from 45 degrees to 0.2 degree. Finally, the slow start experiments, with the input power to cavity increasing gradually up to the reference setting, have been done successfully too.

SUMMARY

The FPGA based digital RF feedback system have been developed and tested with the newly improved software by using DTL2 cavities and waveguides. The accelerating field stability has been successfully achieved.

REFERENCES

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