# PHASE LOCK LOOP AND ASSOCIATED COMPONENTS FOR THE RADIO FREQUENCY SYSTEM OF THE PF STORAGE RING PART-I

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## 1. Introduction

The PF storage ring is designed to store 0.5 A electron beams at an energy of 2.5 GeV[1]. The synchrotron radiation loss is more than 250 kW for the case with wiggler magnet on. The RF acceleration system (500 MHz), consisting of four 180 kW(cw) klystrons and associated systems, are planned to be installed to compensate the power lost by the synchrotron radiation and to give the phase stability necessary to maintain a long quantum life time. Figure 1 shows the block diagram of the RF system which is now under design and construction. We describe here briefly a design outline of the low power level RF system. Results of basic tests for the phase lock loop using electronic phase shifters[2,3] and phase meter[3] are described briefly.

## 2. Outline of RF control system

1) Phasing: to give proper phase combination to each cavity the electronic phase shifters ("$\phi_1$" in Fig. 1) are used for phase adjustments among four RF lines.
2) Klystron phase lock loop ("KLYSTRON PLL" in Fig.1): to maintain the synchronous phase angle constant, the phase of the klystron output has to be stable against various phase changing effects. (PLL can also be achieved using voltage controlled oscillator as described in Part-II.)
3) Automatic cavity voltage control("AGC" in Fig. 1): to stabilize cavity voltage against beam loading effects etc.
4) Automatic cavity tuning: to compensate reactive beam loading and effects due to the temperature change. Tuning control is made by the voltage corresponding to the phase difference between input signal and sampled signal of the cavity ("TUNER LOOP" in Fig. 1).

## 3. Phase shifter/phase meter/PLL

Electrically variable phase shifters are to be used as control elements in feedback loops and to give proper phase angle in the system. Phase shifter of wide variable range was built using varactor diodes employed as the terminating elements of hybrid couplers. Figure 2 shows the phase response as a function of control voltage. Figure 3 is the polar display at 500 MHz showing 360° phase variation with control voltage of 11 volts. Insertion loss was about 7 dB and maximum rate of phase change was 1 deg/100 ns.

Phase meter which produces dc voltage proportional to the input phase difference, having wide dynamic range was designed and built for the klystron PLL and for the cavity tuning loop. Figure 4 gives the block diagram of the preliminary test for PLL which is albe to lock the phase within ±2° with input phase modulation of 160° and amplitude change of 25 dB.

References

1) Photon Factory Design Manual.
2) H. Schwarz, PEP Note 283 (1979).
3) Manufactured by R and K Lab.

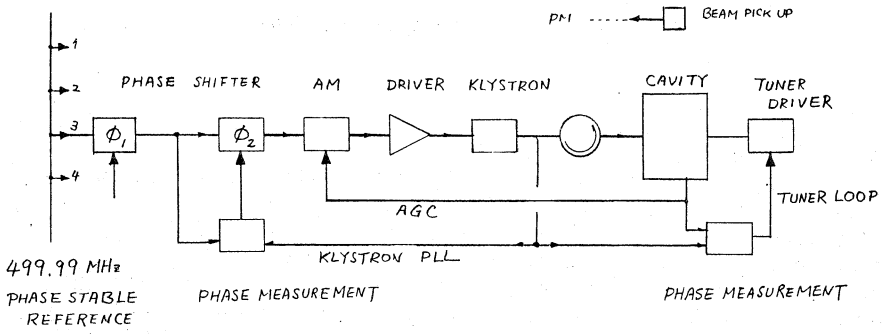


Figure 1 BLOCK DIAGRAM OF RF SYSTEM

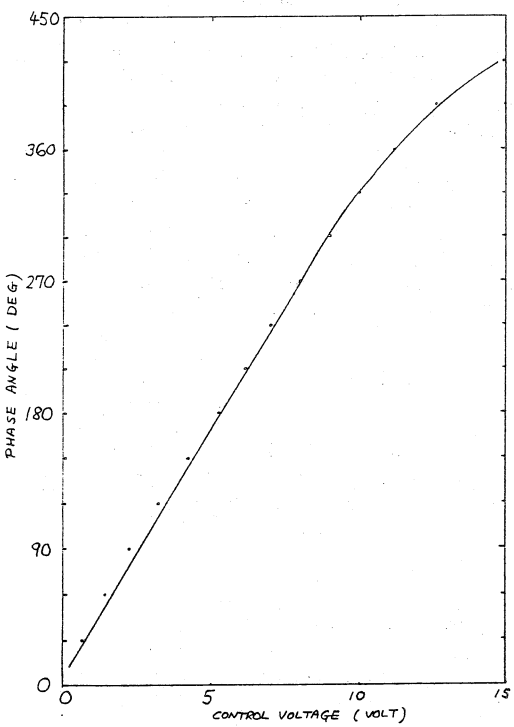


Figure 2 PHASE vs. CONTROL VOLTAGE

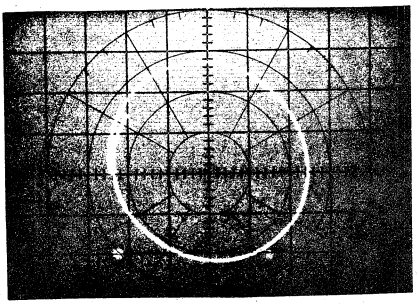

Figure 3

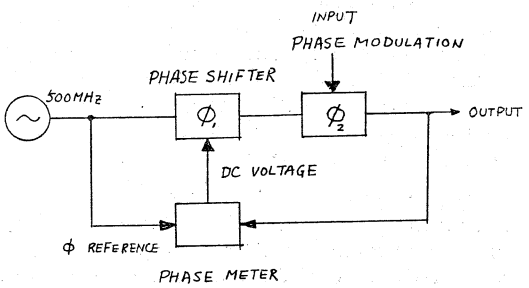


Figure 4 TEST CIRCUIT OF PLL