THE TRIGGER SYSTEM OF KEK POSITRON GENERATOR

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ABSTRACT

The trigger system is in preparation for KEK positron generator now under construction. Outlines and modules of this system are presented.

INTRODUCTION

In the operation of KEK positron generator now under construction several trigger signals are needed for the pulsed operation. The trigger signals are used at a gun high voltage modulator, a gun cathode pulser, klystron modulators, beam monitors and at both of the TRISTAN Accumulation Ring (AR) and the Photon Factory (PF) storage ring which receive the accelerated positron beam.

The maximum of the repetition rate of the trigger signal required for the gun high voltage modulator and klystron modulators is 50 Hz, and the minimum of that is 10 Hz limited to keep the output voltage of the modulators constant. Others' repetition rates are less than or equal to that of the klystron modulators.

To accomplish the single bunch mode operation in the AR and PF ring the synchronization of the triggers with the revolution frequency signal of each ring is needed. Related rf parameters of each ring are shown in Table 1. Since the time interval between bunches in both rings is 2 ns, a short-pulsed beam (shorter than 2 ns) synchronized with 0.79 MHz (AR) or 1.60 MHz (PF) signal in little jitter (less than 100 ps) is requested. In addition the cycle time of revolution is not very small in comparison with the flat top width of the klystron modulator output; therefore the klystron modulator output is requested to be synchronized with the revolution frequency signal.

Table 1 RF parameters of the AR and PF ring

	AR	PF
RF frequency	508.6 MHz	500.1 MHz
Harmonic number	640	312
Revolution frequency	0.79 MHz	1.60 MHz
Cycle time of revolution	1.26 μs	0.62 μs

OUTLINES OF THE SYSTEM

The block diagram of the trigger system is shown in Fig. 1. A similar system is in operation in the PF injector linac.

The 47.6 MHz and 100 Hz clock signal are both derived by dividing the 476 MHz signal from a master oscillator. They are used in the variable delay and in the master trigger generator, respectively. The 476 MHz signal is a master signal of a 2856 (476 × 6) MHz accelerating rf of the positron generator.

In the master trigger generator the trigger-1 which decides a repetition rate of the klystron modulators is made by dividing the 100 Hz clock, and the trigger-2 which decides a repetition rate of the gun cathode pulser is made by dividing the trigger-1 (including no dividing case).

Every output signal of the synchronizer are synchronized with the revolution frequency signal of the AR or PF ring. The ring trigger and the monitor trigger have the same repetition rate as the gun cathode pulser trigger, and go out 100 μs and 1 μs before the gun cathode pulser trigger, respectively. The gun cathode pulser trigger is gated finally by the ON/OFF signal from an operator's console.

The trigger compensator sends out usually the synchronized trigger to klystron modulators, but if it detects lack of that due to a fault of the synchronizer it sends out the trigger-1 not synchronized, and keep the repetition rate of the klystron modulator trigger signal.

The main variable delay is a digital delay which counts the 9.52 (47.6/5) MHz clock signal.

The trigger sub-system is prepared to make a fine adjustment of timing and to set a trigger mode of each klystron modulator.

This sub-system is put in the control room of the positron generator; the synchronizer is in the gun room to reduce jitter of the gun cathode pulser trigger and others of the system are put in the main control room of the PF injector linac. To avoid a false trigger generated by noise in transmission lines between these rooms TTL level trigger pulses are amplified up to 24 V level pulses by a pulse amplifier before transmission.

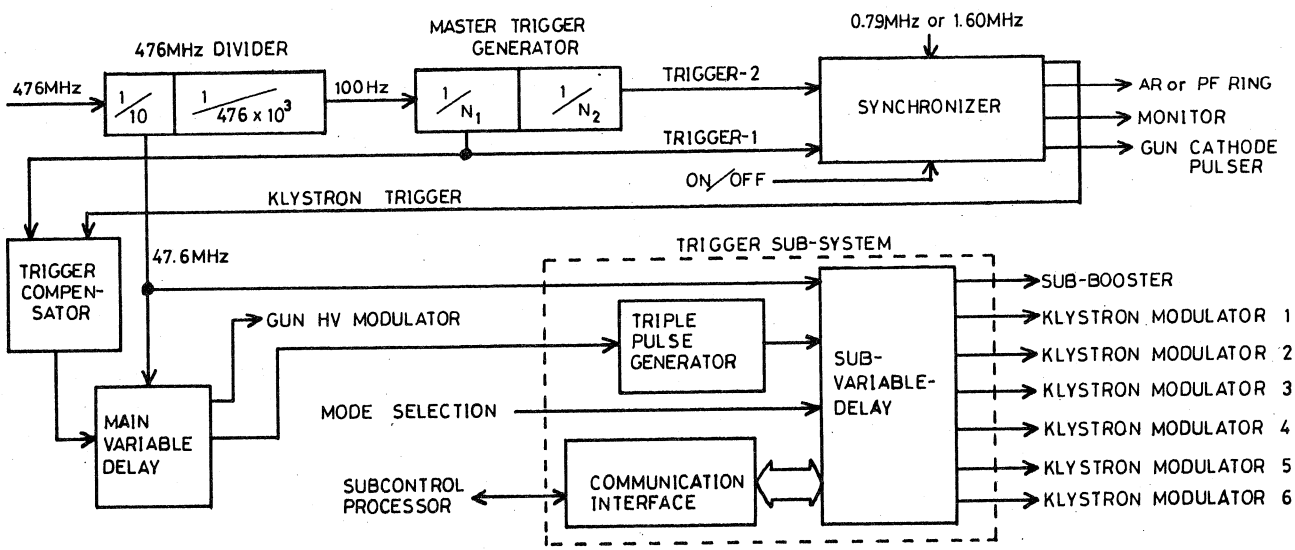

Fig. 1 Block diagram of the trigger system.

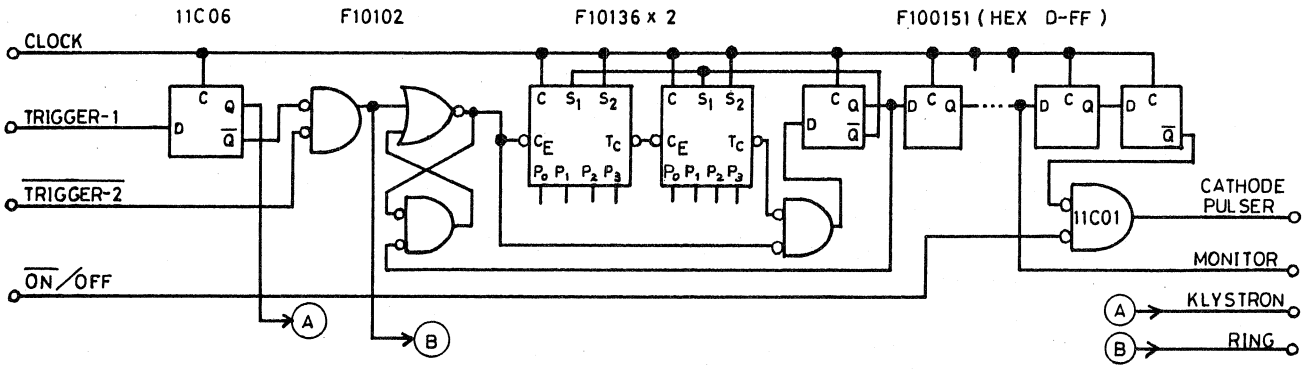

Fig. 2 Circuit of the synchronizer.

MODULES OF THE SYSTEM

476 MHz Divider

This NIM module divides the 476 MHz signal and is composed of emitter-coupled logic (ECL) IC's to treat a high speed signal. If the 476 MHz signal from the master oscillator stops an internal clock generator automatically starts to supply a 47.6 MHz signal instead of the 1/10 divided signal of the 476 MHz clock at the first dividing stage.

Master Trigger Generator

This module is composed of TTL IC's. The trigger-2 signal goes out 10 ms before the related trigger-1 signal and is used in the synchronizer as a trigger of a gate signal to select the gun cathode pulser trigger from the trigger-1 signals after synchronization.

The repetition rate of the trigger-1 can be chosen from among 50, 25, 20 and 10 Hz by means of setting a rotary switch on the front panel of this NIM module. The repetition rate of the trigger-2 can be chosen in the same way from among many values from 1/1 to 1/450 of that of the trigger-1.

Synchronizer

This NIM module is composed of high-speed ECL IC's to get the smallest jitter. The circuit of this module for the PF ring is shown in Fig. 2. The trigger-1 signal is synchronized with the revolution frequency signal by a D-type flip-flop. A delay circuit is composed of two hexadecimal presettable down counters and six D-type flip-flop's (as a six-bit shift register) using a clock of the revolution frequency signal.

For the AR almost the same circuit is used; preset values of the counters and the position of the monitor trigger output are changed from a case of the PF ring injection.

The gun cathode pulser trigger with jitter less than 100 ps is obtained.

Trigger Compensator

If the klystron trigger does not come from the synchronizer into this module after the trigger-1

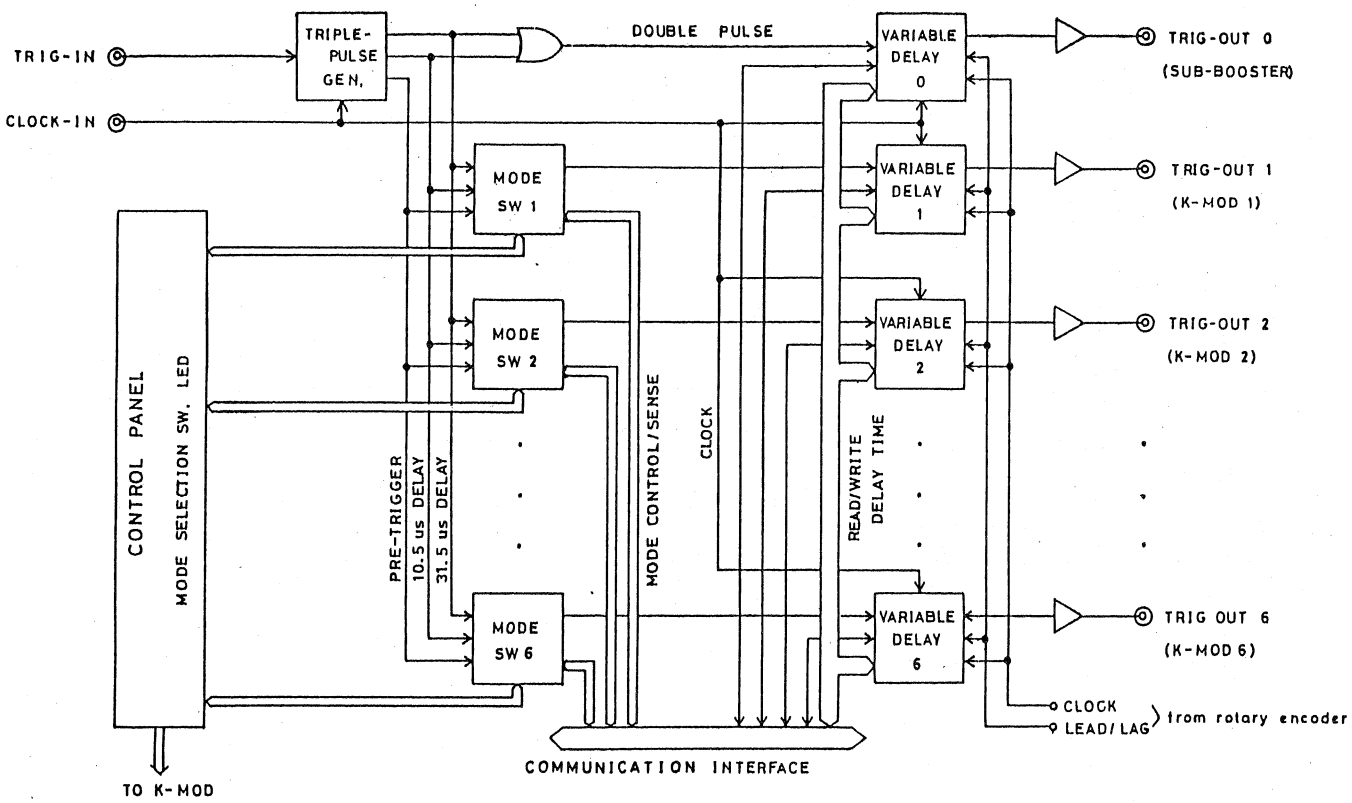

Fig. 3 Block diagram of the trigger sub-system.

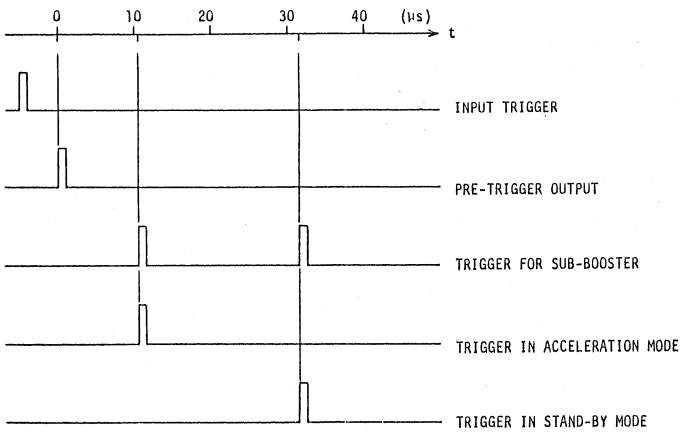

Fig. 4 Timing chart of the trigger sub-system.

comes, the trigger-1 is delayed and sent out. This NIM module is composed of TTL IC's.

Main Variable Delay

This digital delay module composed of TTL IC's uses a 9.52 MHz clock derived by dividing the 47.6 MHz clock by 5; the unit of delay time is 105 ns. Delay time can be chosen by means of setting the thumb-wheel switch from 1 to 99 on the front panel of this NIM module; the maximum delay time is 10.4 μs.

Trigger Sub-system

The block diagram of this sub-system is shown in Fig. 3 and its timing chart is shown in Fig. 4.
Once a trigger pulse is inputted, a triple pulse train is generated. The first pulse of the train is used as a pre-trigger in the sub-variable-delay module. The second pulse 10.5 μs after the pre-trigger is used as an acceleration mode trigger to the klystron modulators. The third pulse 31.5 μs after the pre-trigger is used as a standby mode trigger. In the acceleration mode the beam can be accelerated but in the standby mode it cannot and the klystron modulators fire only to keep the operating condition stable. Both of the second and third pulses are supplied to the sub-booster which is the pre-stage amplifier of the 2856 MHz signal.

The trigger in each mode is delayed in the sub-variable-delay module to adjust the trigger timing for every klystron modulator. The delay unit is a digital circuit which counts a 47.6 MHz clock signal using a 3-digit presettable BCD counter of Schottky TTL. The maximum preset value is 999; the maximum of the delay time is 21.0 μs. The circuit of this module is shown in Fig. 5.

The trigger sub-system is built in a case like a CAMAC crate and can be controlled by the subcontrol processor through an asynchronous communication line with 48 kbps signalling rate as well as by manual operation at the front panel.

Pulse Amplifier

The pulse amplifier unit has 12 channels of inputs and outputs in a 19" rack-mount case.

In the last stage of amplification a MOS-FET is used and the output signal is electrically isolated by a pulse transformer. When the INHIBIT input is short-circuited to ground the signal output is inhibited. The output signal with pulse height of 23 V and rise time of 50 ns is obtained under conditions of 50 Hz and 2 μs width.

We would like to thank Y. Hosono and K. Hasegawa of Faculty of Engineering, University of Tokyo for their useful advice.

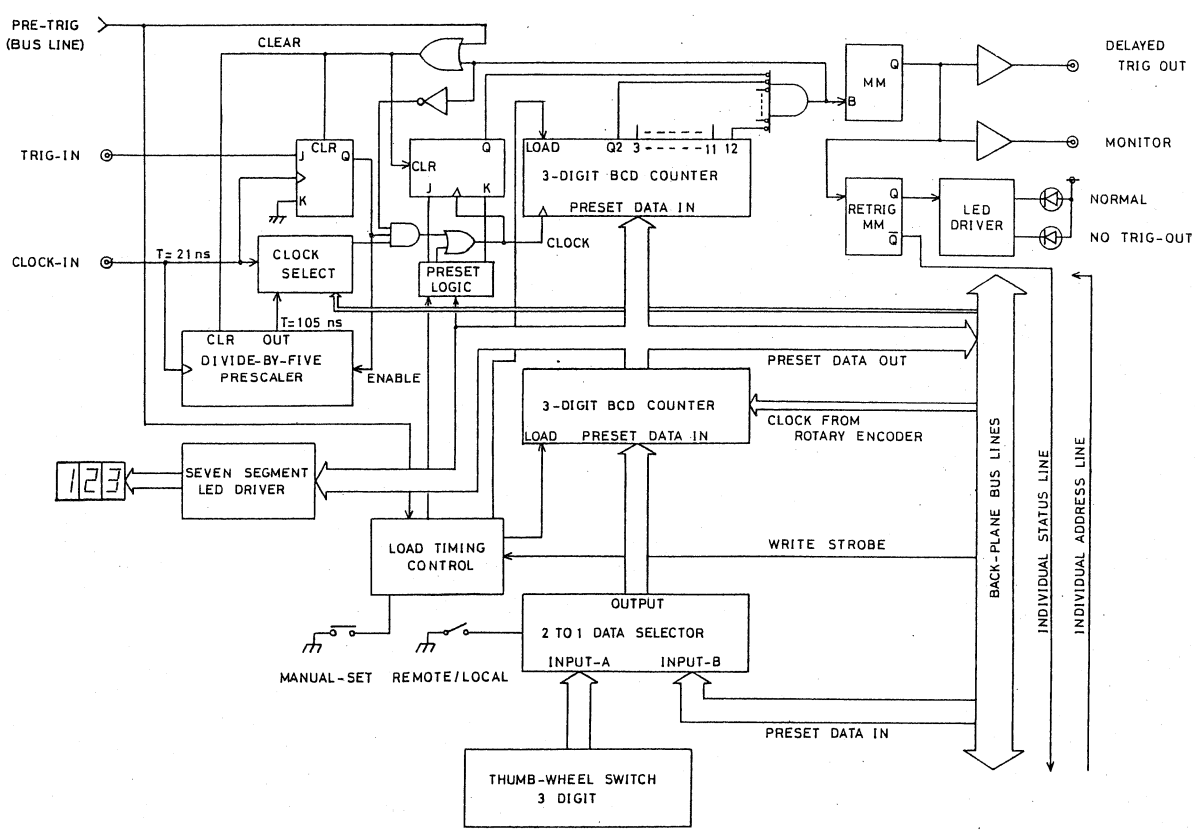

Fig. 5 Circuit of the sub-variable-delay.