TEST SYSTEM FOR KEK PS CONTROL USING VME COMPUTERS AND PRIVATE NETWORK

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ABSTRACT

The control system for KEK 12 GeV Proton Synchrotron will be replaced with a new micro-computer system with a new computer network system. The VME-bus based multi-microcomputer system has been introduced into the test control system. A private network system named 'mini-KOP' for test is a 'token-bus' system with 9600 bps MODEM. Special extended PASCAL program 'OBJP' is also made for network support and simple programming. The OBJP is built from the analysis of control programs.

In this paper we describe the prototype system; the VME-computer construction, the mini-KOP, the OBJP programs and operation of the system.

INTRODUCTION

MELCOM-70 multi-computer system has been used as control computers for 12 GeV proton synchrotron for about 14 years[1]. The system is composed of eight 16-bit mini-computers; a multi-purpose central computer, a data-logging one and six satellite ones. The data logging computer is called 'software development computer', because this is used for programming at early time. Now, the central computer is used both for programming and real-time tasks such as accelerator condition displays, human interface for operation and network control.

Satellite computers have one or two process input/output controllers for data taking and device control. As they have small size memory and poor CPU power, the programs are simple and premitive.

Due to poor CPU power of the satellite computers and heavy duty of the central computer, response of the system is very slow for human interface. Power of the 16-bit mini-computer is limited mainly by memory work space; summation of system program, real-time tasks and a user program is limited to 64 kW. Large scale data analysis program cannot run on this system. Recently, the failure rate of the system has so increased and the maintenance of the system becomes very difficult.

Replacement of the system has been decided related to the reason written above[2]. New system is composed
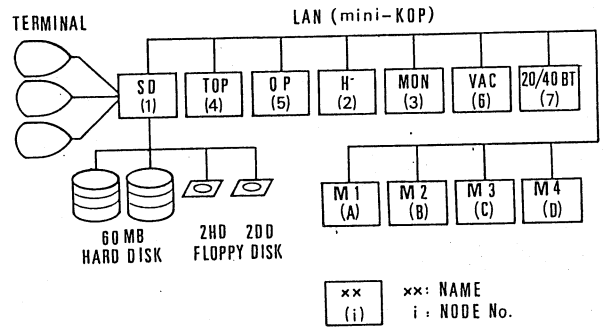

Fig. 1 *Test control system with VME-computers.*

of VME-computers which are widely used standard bus computers. By using VME-computer in standard Euro Card format[3] with reliable two-piece connectors, the system can be constructed to be very flexible and the multi-CPU board configuration is possible.

The test system consists of eleven VME-computers; a software development computer, operation console computers and data-taking computers. They control the 20/40 MeV beam transport line devices, booster injection system power supplies and main ring dynamic steering magnet power supplies.

In the new system, M68000 family CPUs and VERSAdos operating system are used for both real-time control task and programming. The software development computer and satellite computers communicate with each other through a home-made network which is called mini-KOP. The prototype control system is described in this paper.

SYSTEM CONFIGURATION

Eleven VME-computes are distributed around the accelerator as shown in Fig.1. Both 'SD' and 'TOP' are installed in the programming room and other computers are in the control room and sub-control rooms.

A software development computer 'SD' has three terminals, two 60MB hard disks. Three persons can make program simultaneously using the computer, because it is a multi-user system. The 'SD' has both the main CPU board called MVME-121 (MC68010 + MC68451) and a communication CPU board (M68000 family). Fig.2 shows the configuration of the 'SD' system. It has both a graphic display controller and a display monitor for checking the network. Under VERSAdos, both real-time tasks which are related to the network and transient tasks for programming run on about 5MB memory.

Ten satellite computers have no disk memory and no terminal. But they have various process input/output boards; A/D, D/A, digital input/output, graphic display controller, pulse-train gernerator and MIL-1553B like serial device controller. The configuration of the satellite computers are classified by CPU into two types as shown in Fig.3. First generation has an MC68000 CPU on the main CPU board and the second generation has an MC68020 and an MC68881 on the main CPU board. In both generations, the home-made network devices are same.

Both 'OP' and 'TOP' are operation console computers. They have graphic displays and a touch-panel for human interface. We adopted multi-displays insted of multi-windows on single display for simplification both of programming and operation.

The '20/40 BT' controls the all power supplies of the 20 MeV and 40 MeV beam transport lines. A vacuum
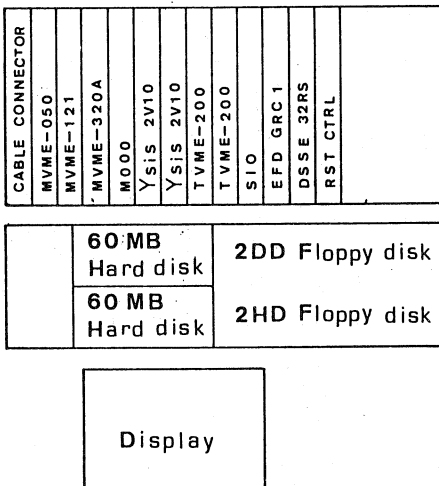

Fig. 2 *Configuration of the software development computer 'SD'.*

CPU   S-RAM D-RAM RS-232C

| MACRO-6001 | MACRO-6001 | Ysis-2V10 | Ysis-2V10 | TVME-200 | SIO | AD, DA, RELAY etc. | FIRST GENERATION |

|— MAIN PART —|— PERIPHERAL —|

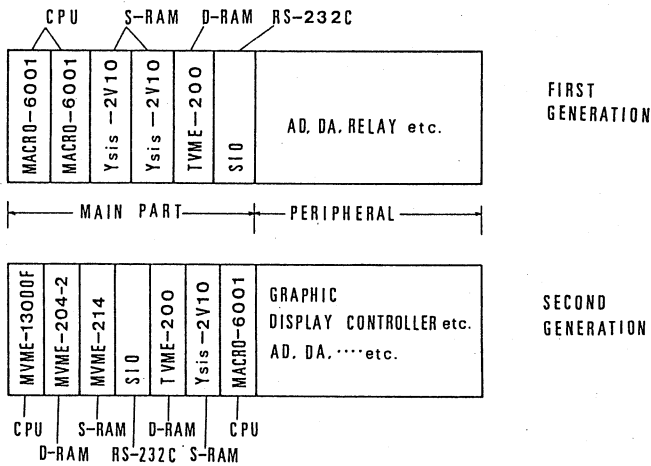| MVME-13000F | MVME-204-2 | MVME-214 | SIO | TVME-200 | Ysis-2V10 | MACRO-6001 | GRAPHIC DISPLAY CONTROLLER etc. AD, DA, ····etc. | SECOND GENERATION |

CPU | S-RAM | D-RAM | CPU
D-RAM RS-232C S-RAM

*Fig. 3 Basic configuration of satellite computers.
In our system of first generation, MC68000 CPU is used. In second generation, MC68020 CPU is used.*

gauge and valve status of the lines are connected to the 'VAC'. The 'H-' controls the power supplies of the booster synchrotron injection magnets for the charge exchnge injection.

The 'M1', 'M2', 'M3' and 'M4' are for control of the power supplies of dynamic steering magnets of the main ring. They will be used for other purpose at each location.

The 'MON' watches the beam intensity signals of all accelerators of the proton synchrotron and takes the data of the 20/40 MeV BT profile monitor.

NETWORK

The each VME-computer communicates through a home-made network (mini-KOP). The network interface of a VME-computer is composed of a CPU board, memory boards, a serial I/O board and an RS-232c modem. The bit rate of network is 9600 bps. The scheme is base-band and token-bus. The token rotation time of the network is about 0.2 second with no data and it depends on the data length.

The maximum data transfer rate depends on the bit rate and is 1kB/second. The maximum number of packet transmission per node depends on the token rotation time, about 4 times per second.

Fig.4 shows the packet frame in the network. In this network, duplicate header method is used for error check of the header. Check-sum method is used for error check of the data part. Most of the frames on the network are with no data and no check-sum part.

The data types of the network are categorized as listed in Table 1. One group is for the communication CPU, the other group is for the main CPU with VERSAdos. New communication program and the VERSAdos which are in absolute load modules are handled by the communication CPU (MACRO-6001 of second generation in Fig.3). Application task modules and messages between tasks are transferred from communication CPU to the main CPU (MVME-130 of second generation in Fig.3) and handled by the main CPU.

Message length of this system is limited to 255 bytes by VERSAdos. But the limit is rather suitable for this system, bacause the network cannot send long messages so fast.

Command and data transfer between the communication CPU and the main CPU is accomplished by passing the pointers and buffers in common memory. On the transmission, a part of the main memory is used as a temporary data buffer. Then the pointer which points to the location of the buffer is set in the pointer buffer in the common memory. On reception, data is stored in the buffer in the common memory and the pointer is set in the pointer buffer.

Both pointers are manipulated by special tasks on VERSAdos. Server task works on transmission by "TRAP #6" command in an application task. Receiver task works every 0.1 second and checks the pointer. If new data has arrived in the buffer, it activates a new task or it sends the message to the destination task.

Table 1 Data types on the network.

TYPE CODE	CPU	DATA TYPE
M	COMMUNICATION CPU	ABSOLUTE LOAD MODULES (S-FORMAT)
Y		VERSAdos (S-FORMAT)
=		=G $XXXXXX START FROM $XXXXXX
L	MAIN CPU	POSITION INDEPENDNT (DISK FORMAT)
Q		MESSAGE TO A TASK

SOFTWARE   -OS and OBJP-

VERSAdos is a multi-user, multi-tasking operating system for the M68000 family CPU in a VME-module made by Motorola. The kernel of the VERSAdos is the RMS68K Real-time Executive which provides task services and supports memory management. It also allows inter-task communication.

The VERSAdos can generate both hard disk operating system and diskless operating system. At 'SD', the hard disk operating system is used. On the other hand, all satellite computers have diskless VERSAdos.

The inter-task communication is expanded for network support by the network server task. In this system, any task can communicate with all tasks in any computer in the network.

Both Pascal and assembly language system are used for programming. Pascal is expanded for network support by a program called 'OBJP'. Fortran is now under test for use in this system.

The programming model by 'OBJP' is shown in fig.5. By the 'OBJP', some routines are built in the task automatically, which are as follows,

1) creates an Asynchronous Service Queue of message receive buffer,
2) "WAIT" for message,
3) selects a subroutine by "message selector",
4) calls a server for message transmission.

When a message arrives at a task, the message comes into the ASQ, then "WAIT" state turns to "RUN" state. At that time, a subroutine called "method" which is selected by the message is executed. After the work of the method is finished, the task returns automatically to the wait state awaiting for next message.

In the 'OBJP', a series of characters

<:=

means message tansfer. A line of text

1:DCLK <:= 'MESS TEST' ;

means that the message 'MESS TEST' is sent to a task 'DCLK' in the computer No.1. When the target task is in
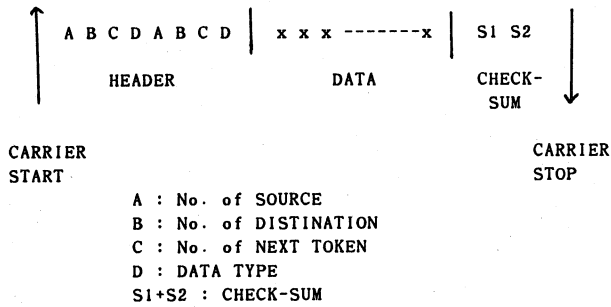
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  ┌─ A B C D A B C D │ x x x ------- x │ S1 S2 ─┐
  │        HEADER              DATA        CHECK-  │
  │                                        SUM     ▼
```

CARRIER   CARRIER
START   STOP

A : No. of SOURCE
B : No. of DISTINATION
C : No. of NEXT TOKEN
D : DATA TYPE
S1+S2 : CHECK-SUM

Fig. 4 Frame configuration of a packet on the network.

the same computer, a mark "!" is used in place of the number. So, text becomes

    !:DCLK <:= 'MESS TEST' ;

Because the 'OBJP' builds automatically some rountines shown above into the pascal program, programmer need not think of communication routines. By the simplification, the programming time is reduced to 20 percent of the time compared to the conventional programming of a short program.

Using 'OBJP' and VERSAdos, each program for control can be divided into small tasks. As the debugging of smaller tasks is easier, programming becomes very easy by 'OBJP'. It is also easy to modify programs. Some tasks can be commonly used by many tasks.

The 'OBJP' also supports a cyclic process. This function is used for the time display, averaging data and cyclic check of status of the accelerator.
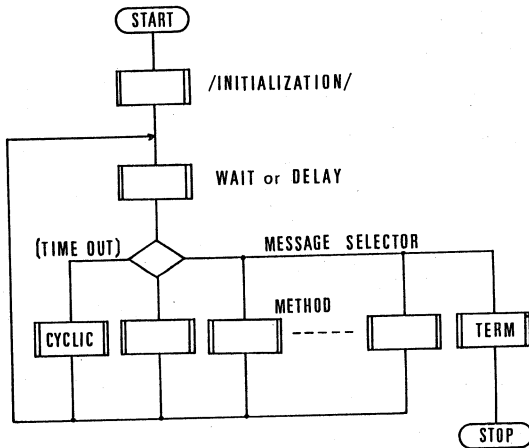

Fig. 5 The flowchart of a task made by 'OBJP'.

CONCLUSION

The prototype of the control system constructed with VME-computers taught us many things, and ---

1) we have got many knowhow about computer control,
2) we found a simple way of programming by using 'OBJP',
3) we have experienced much about VMEbus and VME-computer systems.

A problem about the VME-computer system is that some VME-boards do not satisfy the VME-standard. Some VME-boards in our system often occurred troubles due to above reason. The rate of CPU-halt has been decreased, after some bad boards have been improved. Some troubles may still remain on some boards. Therefore, we should use the VME-boards that are certified by the test facility of the VME products.

The improvement plan of this system is,

1) Raise the bit rate up of the network to 10Mbps.
2) Minimize errors in data transfer.
3) Upgrade of the CPU from MC68000 to MC68020.
4) Intelligent I/O controller for process control.
5) Better man-machine interface.

Now, we are replacing the mini-KOP to the MAP, which is 10Mbps token-bus local area network[4]. Then the system will become enough powerful to control the accelerators.

ACKNOWLEDGEMENT

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