Synchrotron Control System of the HIMAC

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Abstract

A structural design synopsis and the present status of the HIMAC synchrotron control system are described. The control system comprises of Timing System, (ring magnet) Power-supply Controller, Programmable Logic Controller, Static Var Compensator controller, Monitor Controller, RF control computer, Beam Transport control computer and the synchrotron main computer (denoted as CS, hereafter) that forms a local area cluster with man-machine interfacing computers, and communicates with HIMAC supervisor computer.

I. INTRODUCTION

The framework of the control system of the HIMAC synchrotron was reported in the previous symposium[1]. As the HIMAC[2], medical heavy ion accelerator complex, is in the final stage of assembly, it is quite appropriate to describe the organization of control system.

The central issue of the system is the tracking control of the synchrotron lattice magnets, BM and QF/QD. Since the lattice magnets are excited by thyristor power supplies, output control of the latter should be carried out in synchronization to the thyristor control pulses. Various event pulses should also be derived from the same clock. This concept defines timing system. RF system must be operated in coordination with main magnet excitation pattern. It must be noted that there are so widely variant objects of control; from a beam detector of pico-ampere range to a power supply of thousands' amperes; from vacuum pumps to chamber gas handlings. As the operation of the synchrotron is carried out by operators who also run the other machines, procedures for sequences and individual manipulations should be common to all the subsystems (injector linacs, synchrotrons, and the beam transport lines) in man-machine interfacing layer.

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II. SYSTEM COMPOSITION

Figure 1 shows the schematic diagram of the synchrotron control system.

A. Timing System

The base clock is a 1200 Hz that is generated from the Phase Locked Loop of the 50 Hz power line. The master clock that defines the synchrotron operation cycle also synchronizes to the zero-crossing of the U phase of the power line. The system is made up by the PLL, the clock signal distributor CLK10, and the VME subsystem (TS) which includes cpu crate and i/o interface crate. Each ring has its own system except, of course, PLL that provides the common base clock.

The TS generates event signals for Injection, Capture, Acceleration, Flat-Top, Extraction etc., which are written in pattern memory of FDO modules and controlled by the same system that controls pattern power supplies. The TS also delivers switching and other command signals to the FDO's of the power supply controllers.

Typical VME cpu crate consists of MVME147S-1 cpu (68030, 25MHz), HIMV-210 memory (2MB), Ethernet I/F, and RAS board together with Process I/O boards. In TS, DR104 delay repeater modules are used to control the event timing signal in a microsecond precision.

B. Power supply Controller

The Power supply Controller, PC, is also a VME system which is similar to the above mentioned TS in module configuration and operations. The main ingredient of PC in hardware is the FDO, Fast DO, that commands output current and other patterns to pattern-operated power supplies. It has a dual memory and a digital signal processor, DSP56001, to manage real-time operation of the pattern output and memory switching.

For main magnets, a control method that exploits repetitive nature of the synchrotron cycle is introduced to achieve stable and effective operation of the synchrotron.[3] It requires corresponding FDI and massive data processing in

VME system. In fact, there are 3 FDI's and 4 FDO's for BM, and 3 FDI's and 3 FDO's for QF (same is for QD), since V, not only I, pattern is to be controlled. To utilize the programming capacity maximally, PDOS real-time OS is adopted and application softwares are developed on a workstation (SPARC) environment.

C. Programmable Logic Controller

Since the load of PC for numerical control is considerable, we put the task of On/Off control and status check including error detection of the ring power supplies to the PLC, which is regarded to be more robust and less expensive than micro-computers. As such, HIDIC-S10 series of Hitachi is employed. The cpu, S10-2α, is 68000, and can perform up to 28K ladder steps in about 30 ms. I/O points amounts to about 500 for each ring at present.

D. Static Var Compensator controller

The Static Var Compensator can be operated in either analog or digital control mode. The SVC controller is a VME system that outputs the pattern for digital control of the SVC in the same manner as the PC does for each power supply.

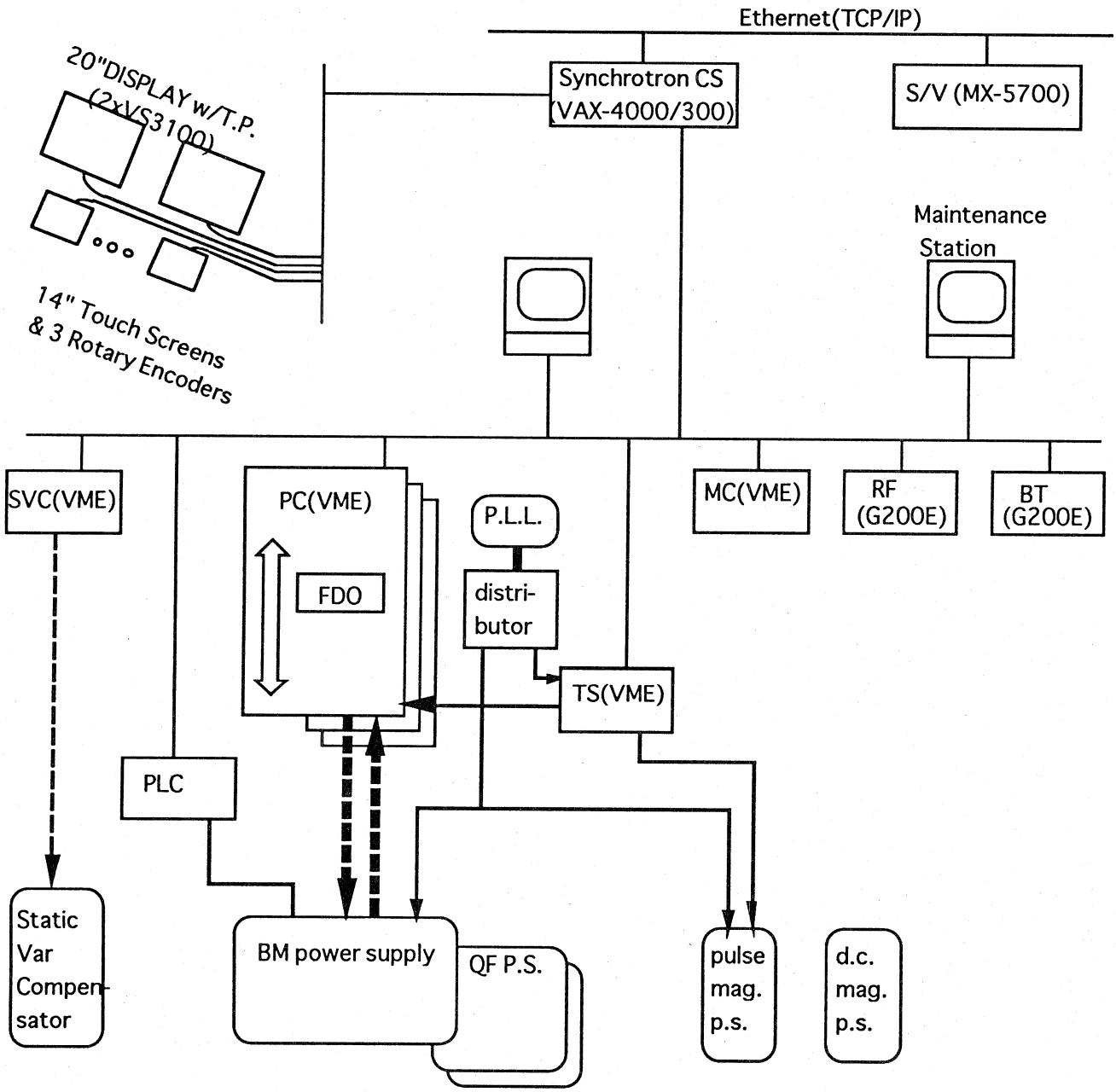

Fig.1 Schematic diagram of the HIMAC synchrotron control system for one ring. Connection between computer nodes is drawn to show an entire system configuration. The representative power supplies and relevant signal flow are depicted additionally to give an idea on functions.

E. Monitor Controller

Monitor controller takes care of the profile monitors and some of the other beam instrumentation. The positioning of the static deflectors is also carried out through this VME system. Along with usual DIO modules (HIMV605, 605AT), it includes Analog I/O (VMIVME3101/4120) and GPIB interface (EVME-GPIB21). As a Relay output module from abroad failed to work appropriately, alternative has been configured with HIMV604A and OMRON G6B-4ND.

F. RF control computer

The control of RF accelerating system is characterized by digital technology and feedback mechanism within the system devices.[4] The faster T-clock (50 kHz) and 0.2G B-clock, together with a larger pattern memory than magnet control is also to be noted. Toshiba G200E computer is the RF subsystem process controller, which also monitors the ring vacuum status and controls vacuum equipments, because Toshiba is in charge of these systems. It also covers the readout of pick-up beam position monitors which uses the same technique as the position monitors in the RF feedback system.

G200E is an FA machine which uses the i80386 (25 MHz) cpu and the AT bus, and is operated under the vendor's version of 'realtime' UNIX. For Process I/O, 5800 series of Toshiba is adopted, and about 10 each for input and output cards (16 points per card) are installed. RS232c and GPIB interfaces are needed for RF timing system and the pattern memory, respectively.

G. Beam Transport control computer

Beam lines just before and after the ring are also controlled by a G200E system that is similar to RF one. I/O points, however, are much larger (1600-2000) due to the beam line magnets whose output control and monitoring are done in 16bits. For example, the injection beam line for the lower ring has 3 bending magnets, 19 quadrupoles, and 9 steering magnets, together with monitors (profile and intensity) and vacuum systems.

H. Man-machine interfaces

As mentioned in the beginning, system should be consistent with the other systems. This request dictates the feature of the man-machine interface: Two 14" displays, two 20" graphic displays, both with touch panels, and three dial knob rotary encoders. Efforts are made to standardize display format and touch-command sequence for the operator. However, because specific function, e.g., pattern editing, is necessary for synchrotron operation, additional feature is prepared and input using a mouse is partly possible.

I. Main control computer (CS)

For the main computer, VAX4000/300 is installed as was already described in Ref. 1, although the interfacing between monitors via GPIB and RS232c is transferred to the MC. An RDB is introduced to manage operation parameter files with patterns. The communication to the supervisor computer (MX5700II, Mitsubishi's UNIX machine) has been established with TCP/IP protocols.

III. PRESENT STATUS

One of the major concern in this kind of system is the traffic throughput of the network. A series of preliminary test with a simulated environment was executed and the resulting collision delay/loss seem tolerable. However, it remains to be seen whether the system endures in the actual operational situation.

As of June 1993, all the hardwares have been installed and the final phase of the connection and coordination testings among the sub-systems of various manufacturers are under way. We anticipate that the system will be ready for commissioning works later this year.

IV. ACKNOWLEDGEMENT

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