FIR Filters for the Bunch-by-Bunch Feedback System of TRISTAN II

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Abstract

A digital filter can be the central unit for signal processing in the bunch-by-bunch feedback system for the TRISTAN II B-factory. Due to the 500-MHz high bunch frequency (2 ns inter-bunch intervals) and the large bunch number of about 5000 for TRISTAN II, we should choose a processing scheme that might be simpler and less expensive to build the electronic hardware required to implement the feedback filter and to reduce the scale of the MACs. The performance of such a simplified system should not be greatly reduced. This paper compares different FIR digital filters so that we can choose the one most suitable for TRISTAN II. These proposed digital filters are very simple, yet can satisfy the basic requirements required of them.

1. Introduction

In the B-factory, thousands of bunches will be stored in rings in order to obtain a very high luminosity. That should inevitably introduce a serious problem involving a coupled bunch instability. How we can suppress the coherent oscillation of bunches is one of the serious problems which must be solved. The design of a bunch-by-bunch feedback system is not easy, because the bunch spacing is very short. In the case of TRISTAN II, the bunch spacing will be only 10 ns even in the earlier stage. It will be shortened to 2 ns during the final step of the project. We are now making a consistent design of the feedback system.

The feedback system comprises three parts: an oscillation-detecting part, a signal-processing part and a kicker part. The main tasks of the signal-processing part are:

- to suppress the DC component and noise contaminating the input signal from the oscillation-detecting part;
- to provide the required feedback gain and a proper phase shift at the oscillation frequency.

These requirements describe a bandpass filter. The filter for signal processing can be realized by either an analog or digital approach. The latter seems to be more attractive due to thousands of circulating bunches and short interbunch intervals for the B-factory accelerator [1,2]. In this paper we discuss some options for the digital feedback filters.

2. Proposed Digital Filters

There are two types used in digital filtering: finite-impulse response (FIR) and infinite-impulse response (IIR). Here, we restrict ourselves to the former. In general, if an FIR filter has an impulse response of $h(0), h(1), \ldots, h(N-1)$, and $u(k)$ represents the input of the filter on sample k; the output $y(k)$ on sample k is given by

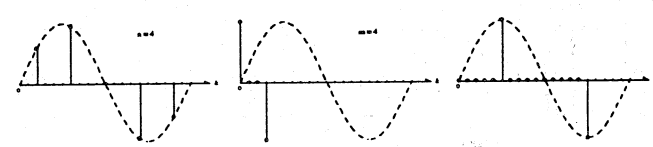
$$y(k) = \sum_{n=0}^{N-1} h(n)u(k-n), \qquad (1)$$

where N is called the number of taps (or coefficients). We divide FIR filters into three groups based on the method used to determine the filter coefficients:

- downsampled mode;
- differentiator mode;
- peak gain mode.

This kind of division is not quite appropriate, since the differentiator mode digital filters mentioned below are not exactly differentiators. Strictly speaking, differentiation can be defined only for a continuous-time signal. Thus, by a digital differentiator we mean a digital filter whose characteristics are similar to those of a continuous-time differentiator [3]. From this point of view, the peak gain mode and downsampled mode filters can also be regarded as being differentiators in a given frequency range.

The concept of dowmsampling (some calls it subsampling [4]) and the proposed downsampled FIR filter can be found discussed in many papers [5-8]. Some descriptions of the differentiator mode and peak gain mode FIR filters are given in Reference [9]. The main difference between the downsampled mode and the other two modes is that the sampling frequency of the former is f_0/n, where f_0 is the revolution frequency of the bunch and n is the downsampling factor, while the sampling frequency of the later is the full revolution frequency. The number of taps of the downsampled FIR filter is $N = 1/(n \times \nu_s)$ for the longitudinal feedback system, where ν_s is the synchrotron tune.



(a) Downsampled (b) Differentiator (c) Peak Gain

Figure 1: Impulse Response of FIR Filters

Figure 1 shows examples of the unit impulse response of FIR filters for these three modes. The dashed lines in the figure indicate one cycle of the synchrotron oscillation. One of the design values of TRISTAN II is $f_0/f_s = 1/\nu_s = 20$. For the downsampled mode FIR filter, the sine-shaped envelope of the sequence of the impulse response $h(k)(k = 0, 1, ..., N-1)$ is not necessary. It can be any shape, such as triangular or square wave. But, a sine wave makes the filter more easily to satisfy the requirement of DC rejection, i.e., $\sum_{k=0}^{N-1} h(k) = 0$. Though there

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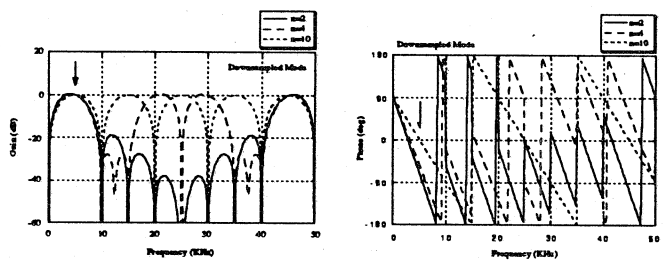
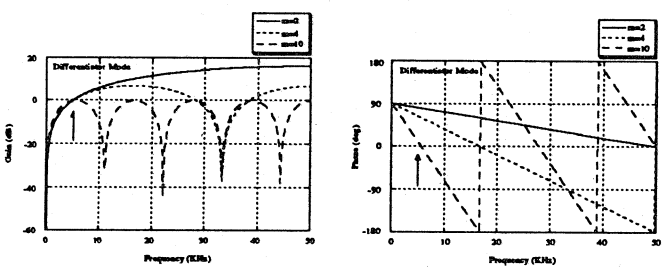
are 4 and 16 coefficients for the filters shown in Figures 1-(b) and -(c), respectively, only 2 coefficients have non-zero values for both cases. We sometime call them 2-tap, but not 4-tap or 16-tap FIR filters. Figure 1-(b) shows the $m = 4$ case, where m is the number of memories per bunch to be used. m can be any number from 2 to 10 for the $1/\nu_s = 20$ case of TRISTAN II.

3. Comparisons

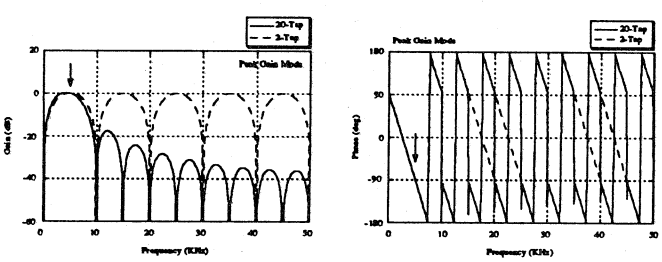
Figure 2 shows the frequency response functions of the filters for each mode. To make comparisons, all filters were selected to have the same 0 dB gain at the synchrotron oscillation frequency $f_s = 5$ KHz. The arrows in the figure indicate the synchrotron oscillation frequency f_s. From the figure we can see that all demonstrated filters provide the required DC rejection, and all of them are a linear phase shifter. The bandwidth of the filter is widened with a decreased tap number N and memory



(a) Downsampled Mode



(b) Differentiator Mode



(c) Peak Gain Mode

Figure 2: Frequency Responses of FIR Filters

number m of the filter. This means that a short-length digital filter passes more noise signals above the synchrotron oscillation frequency. Differentiator mode filters have a higher gain at the high-frequency region than at the synchrotron oscillation frequency. The peak value of the gain increases with decreasing m, and occurs at a frequency of $\frac{f_0}{2(m-1)}$. For a filter with a smaller m, its frequency response is closer to that of the ideal differentiator. Actually, the ideal differentiator is a highpass filter. We can also see from the figure that both the downsampled mode and the peak gain mode FIR filters will lose gain if the synchrotron oscillation frequency f_s is not perfectly matched to the center frequency of the filter, while the gain of the differentiator mode FIR filter will increase (or decrease) with increasing (or decreasing) f_s. The phase is more sensitive to the variation of f_s for the peak gain mode FIR filter. It is ± 18 degrees for a variation of $\pm 10\%$ in f_s.

At the end of this section we list the main parameters of the FIR filters for these three modes in Table 1.

Table 1: Comparison of Different FIR Filters

Mode	Diff.	Peak Gain		Downsampled		
Downsampl. factor, n	1	1	1	2	4	10
Sampling freq. (KHz)	100	100	100	50	25	10
Number of taps, N	2	2	20	10	5	2
Phase shift at f_s (deg)	81∼9	−90	−90	−90	−90	0
Group delay (μs)	5∼45	100	100	100	100	50
MACs/s ($\times 10^8$), M	10.24	10.24	102.4	25.6	6.4	1.024
Memories/bunch, m	2∼10	16	20	10	5	2

The MACs per second M in Table 1 is calculated using the following formula:

$$M = \frac{N \times B \times f_0}{n}, \tag{2}$$

where $B = 5120$ is the number of bunches for the TRISTAN II design.

4. Simulations

The computer-simulated input and output waveforms and their FFT are shown in Figures 3–5 for each mode. The input is a 5 KHz sinusoidal signal with $\pm 10\%$ full-scale random noise. It can be seen that the amplitudes of some high-frequency output components of the simple length filters are enlarged due to a wider bandwidth, but the fundamental at an f_s of 5 KHz is not much affected for all cases.

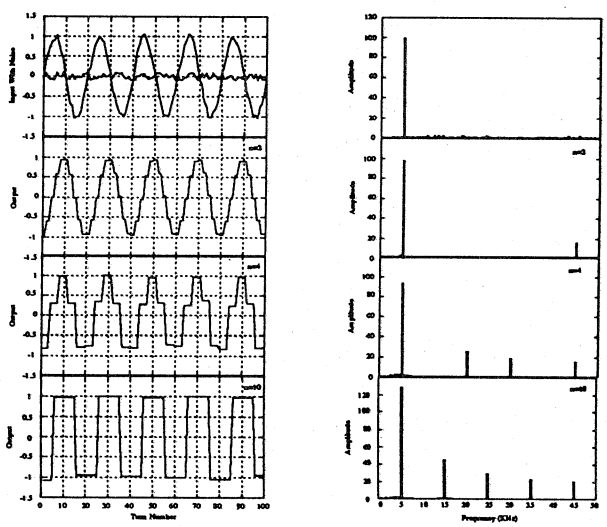


Figure 3: Input and Output Waveforms and Their FFT of Downsampled Mode FIR Filters

In the simulations, the input sinusoid is sampled at around its peak value for the $n = 10$ downsampled mode FIR filter.

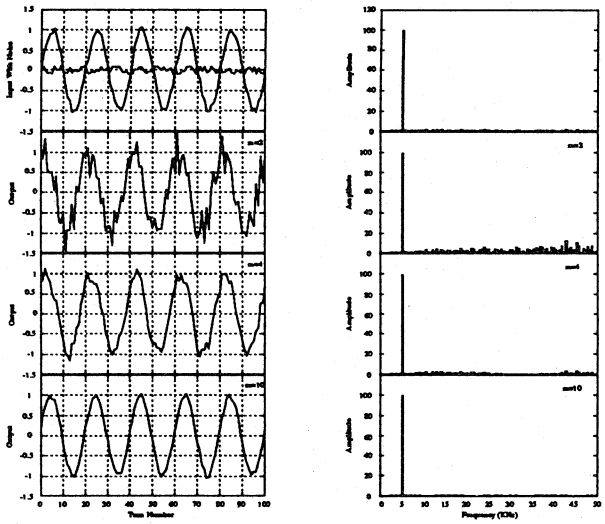


Figure 4: Input and Output Waveforms and Their FFT of Differentiator Mode FIR Filters

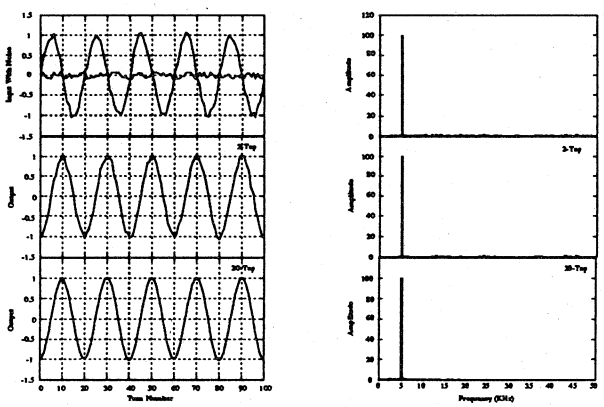


Figure 5: Input and Output Waveforms and Their FFT of Peak Gain Mode FIR Filters

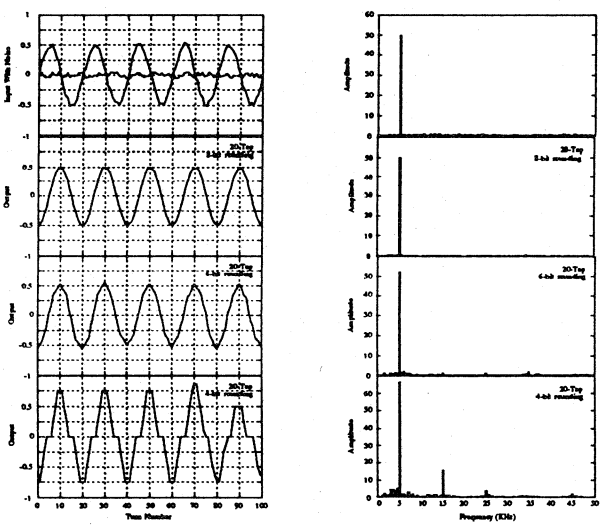


Figure 6: Output Waveforms and Their FFT of a 20-Tap FIR Filter with Finite-Word-Length Effects

Since this can not be guaranteed in real applications, using two samples per cycle of the synchrotron oscillation is not reliable (sampling exactly at the zero crossings of the sinusoid could give no signal).

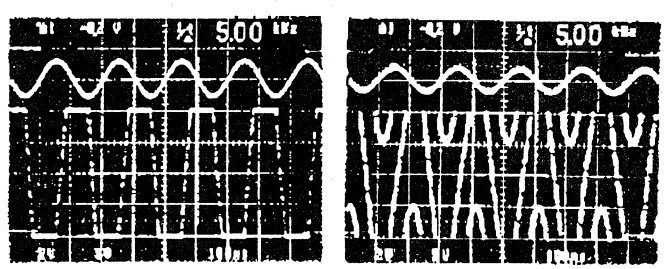
We did not consider the so-called quantization error in the previous simulations. This error is clearly proportional to the quantization step. The quantization step of the general-purpose digital computer, which we used for the simulations, can be as small as 2^{-32}. The quantization error is thus practically equal to zero. If a digital filter is implemented by using special hardware, the number of bits is often limited to from 4 to 16. In this case, the quantization error can no longer be neglected.

Figure 6 is a simulation result for the 20-tap peak gain mode FIR filter after considering the quantization error with a different word length. The input is the same signal as it was before, except that the amplitude is reduced by a factor of 2. The number is represented in fixed-point and 2's complement coding, and is approximated by rounding it to its nearest quantization level. The rounding took place in the following cases: analog-to-digital conversion, representation of filter coefficients, and arithmetic operations. From the figure we can see that the output of an 8-bit word length is sufficient. It is also reasonable to obtain commercially available high-speed components with an 8-bit word length from the current market.

5. Hardware Implementations

The basic components for a digital filter are a delay unit, an adder and a multiplier. The delay unit is a kind of memory element, such as a storage register. The clock synchronizes the movement of the data through the filter.

The hardware implementation of the FIR filter can be achieved by using either the digital signal processor (DSP) or some discrete logical IC chips. Both selections have their own advantages and disadvantages. For example, by using the DSP, the coefficients of the filter are programmable. It can provide a flexible feedback algorithm and can program for several operating modes. It also allows one to implement compact software output limiting, which may need to pay more efforts to realize by using hardware. Figure 7 shows oscilloscope photos of the ADC input (upper trace) and the DAC output (lower trace) of an FIR filter with and without software output limiting.



(a) With Output Limiting (b) Without Output Limiting

Figure 7: Input and Output Waveforms of an FIR Filer With and Without Software Output Limiting

Though the DSP is a microprocessor especially designed for digital signal processing, it is still a kind of a processor driven

by software. It needs some overhead instruction cycles associated with getting data into and out of the DSP, as well as maintaining data buffers and pointers. Because this overhead is independent of the number of taps (filter coefficients), the very short FIR filters turn out to be less effective at reducing the total computation load of the filtering process. Moreover, the complexity of the electronics hardware and the large number of DSPs needed to be used in the system make it relatively high cost and hard to build.

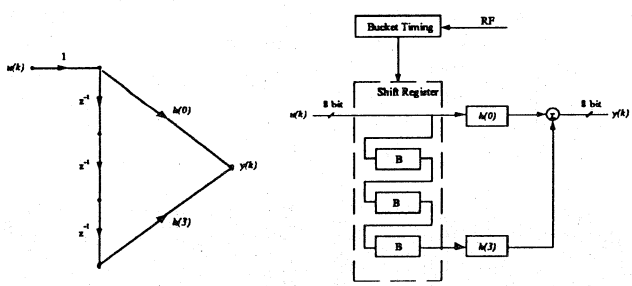
If we use discrete IC chips to implement a short FIR filter, that would be simple. For example considering an actual implementation of a 2-tap differentiator mode FIR filter with $m = 4$, the transfer function of the filter is

$$H(z) = \frac{Y(z)}{U(z)} = h(0) + h(3)z^{-3}, \tag{3}$$

with $h(0) = -h(3)$. The unit delay time z^{-1} is the revolution period of the bunch, T_0. Taking the inverse z-transform of the Equation (3) yields

$$y(k) = h(0)u(k) + h(3)u(k-3). \tag{4}$$

The most common structure used to realize Equation (4) is the tapped-delay or direct-form realization shown in Figure 8-(a). If the speed of the digital components to be used are sufficiently fast, each bunch can be treated separately, but identically, within a bunch spacing of $T_B = 2\ ns$. Therefore only one FIR filter is needed, but the unit delay time should be T_B. Figure 8-(b) shows a block diagram of the filter, where B in the figure is the number of bunches. Because only two coefficients of the filter have the same absolute value but opposite sign, the filter circuit can be further simplified by eliminating the multipliers and substituting the adder with a subtracter. The loop gain of the feedback system can be adjusted using some other methods, such as a multiplying DAC or an analog amplifier after the DAC.



(a) Signal Flow Graph (b) Block Diagram

Figure 8: Direct Form of the 2-Tap Differentiator FIR Filter

Unfortunately, we didn't find an 8-bit high-speed ALU chip which can finish the multiply/add operation within 2 ns until now. We must use a wideband multiplexer and demultiplexer to convert the sequential 500-MHz data stream into several slower parallel streams.

By carefully considering the architecture of Figure 8 we found that there is a problem, i.e., 15,000 high-speed shift register chips must be used because of the ~5000 bunches of TRISTAN II. It is impossible to realize a filter physically with so many IC chips in such a fast electronics system. One solution is to substitute the shift registers with high-speed, large-scale memory chips, such as FIFO. However, the timing and addressing have to be resolved.

6. Conclusions

We compared FIR filters with different tap numbers N and memory numbers m for three modes. The simulation results indicate that all of these filters can be used for TRISTAN II, except for the 2-tap downsampled mode FIR filter. The authors are more interested in the differentiator mode filter with $m = 3 \sim 5$ or the downsampled mode filter with $N = 5$ $(n = 4)$, because of their reasonable MACs per second and memory number which can be used. The results also indicate that 8-bit components can be satisfied. It seems to be attractive to implement a short digital filter by using discrete logical IC chips.

The computer simulations were performed only on FIR filter, itself. That is far from enough. Simulations performed on the entire bunch-by-bunch feedback system are presently being carried out. However, we should test the digital filter algorithm using not only simulated input signals, but actual signals that are representative of the expected bunch-by-bunch feedback system environment as well.

Though the discussions were based on the longitudinal direction in this paper, those proposed digital filters can also be used for a transverse bunch-by-bunch feedback system after some modifications of the filter parameters.

7. Acknowledgements

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