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Development of Dynamic Pattern I/O Modules for Advanced Accelerator Operation

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Abstract

Dynamic control of beam parameters (energy, C.O.D. etc.) is essential for advanced utilization of synchrotron beam. DPI/DPO modules are now under development to switch among various excitation patterns of main magnets and rf system while the synchrotron is operating.

DPI/DPO are VMEbus modules which provide maximum 20-bit parallel input/output port with independent 16-bit control signal port, where up to about 125kHz external clock is applicable. Dynamic switching of output pattern and other intelligent functions are performed by two RISC microprocessors, one for control and the other for calculation.

1. INTRODUCTION

Operation of synchrotron magnets are characterized by repetitive pattern which consists of injection, acceleration, extraction, deceleration and reset of beam. In order to accelerate the beam without losses, each field of lattice magnets, BM and QF/QD, should be excited in a matched strength. This is called as "tracking". Power supplies of lattice magnets, accordingly, should be precisely controlled in synchronization with the 1,200Hz trigger timing pulse of 24 phase thyrister converter for forcing power source.

HIMAC has already made use of FDI/FDO modules which were developed for this purpose [1]. Present control system of magnet power supplies works well, including event triggers that are generated from another FDO module for injection etc. However, an advancement in heavy ion therapy requires more flexible and dynamic control of synchrotron operation, as the beam delivery with pulse-to-pulse energy shift is envisaged for cancer treatment irradiation of three-dimensional scanning for HIMAC and Particle Therapy Project in Hyogo prefecture [2].

An rf system should also be operated in coordination with main magnet excitation pattern, but the clock system differs from that of main magnet power supply. T clock of about 50kHz and B clock of max. 120kHz are used for rf control. Further, B clock is of bi-directional operation to stand with fluctuation of magnetic field for both acceleration and deceleration of beam. Although the dual memory mechanism is utilized and the digital control system operates successfully [3], dynamic pattern switching is not fully realized.

Dynamic switching of these patterns (both magnets and rf) is demanded in various aspects of beam operations. For example, it is required to switch an arbitrary combination of magnets simultaneously during beam tuning or to use a set of excitation patterns as mentioned above. Usage is also expected to measure beam parameters, chromaticity *e.g.*, to initialize magnets, and to achieve digital feedback control (Iterative control or Self-study control).

Thus a dynamic pattern switch/selection is inevitable in advanced synchrotron control, which is now possible with the help of recent high-performance processors. In order to select various excitation patterns of main magnets and rf system dynamically, DPI/DPO modules are now under development. This paper describes DPI/DPO modules, with emphasis on the hardware aspect of DPO, which is developed prior to DPI.

2. FEATURES OF THE DPO

A lot of high performance RISC microprocessors for embedded system has flourished in a wide range of electronic appliances. After our investigation of abilities to handle many external interrupts and to control timer/counter substantially, we have made a choice of Hitachi Super-H (SH) series CPU which uses a 32-bit RISC core optimized for high speed and low power consumption. Another advantage of SH-1 CPU is several on-chip peripherals to eliminate many additional devices.

For a dynamic selection of a required excitation pattern from several tens to hundreds of patterns, it is necessary to discriminate many commands and to prepare enough amount of memory to store all relevant data. For this purpose 12-bit external control signal and 16MB memory are employed.

VSBbus is the subsystem standard of VMEbus.

It is provided to form a digital feed-back loop by interconnection between DPO and DPI, which is expected to correct C.O.D., for example, in real-time. Iterative control of magnet power supplies [4] will be also benefited by the DPI-DPO direct connection.

Table 1 shows the outline specification of DPO. And the block diagram is shown in Fig.1.

2-1. CPU and Memory

Multiple CPU system is provided for this module. SH-1 CPU serves to control communications with VMEbus, VSBbus and all input & output ports. SH-1 also manages SH-2 CPU which is provided for dedicated calculation. To avoid bus contentions of multiple CPU system, separate local bus is provided for each CPUs.

16MB DRAM will be used in 3 byte-word format pattern memory to cover system requirement of rf and BM operation. User supplied programs can be loaded into the DRAM of SH-1 or the dedicated SRAM of SH-2 and executed from local CPU, respectively.

Each CPU responds to commands and environment parameters placed in each 32kB dual ported SRAM which serves the accesses from the VMEbus or the local bus through the arbitration logic which intervenes synchronously with one for another when simultaneous accesses occur.

SH-2 is provided on the mezzanine board to be changeable to SH-3 CPU in future.

Input/output ports are also provided on the other mezzanine board in order to change RS485 to TTL or other interfaces.

2-2. External clock

4 bits are provided for external clocks.

- Pattern start signal (Master Clock or Rf Capture)
  It corresponds to repetitive cycle of synchrotron operation, typically ~1Hz.
- Base clock (1,200Hz or 50kHz)
  1,200Hz is fundamental clock distributed from PLL.
- Incremental B clock for rf (B+ clock)
- Decremental B clock for rf (B- clock)
  Maximum speed of B clock is presumed to be 120kHz in order to cover the BM excitation rate of 2.4T/sec at 0.2G/pulse clock.

2-3. External control signals

12-bit signal is decoded and recognized as following various events. These events are executed after next Master Clock except for Change signals that are executed immediately.

- Start & Stop
  Command to start or stop pattern output/input to devices altogether.
- Pause & Rerun
  Command to break temporarily or rerun pattern output for measurement of beam life etc.
- Selection of pattern
  Command to select any excitation pattern. Decoding method is effective to expand the range of selection, although a surplus strobe signal is necessary. It is capable to select not only any single excitation pattern but also a set of patterns and to operate partly any grouped magnets by means of masking bit, of which feature is applied to Start or Stop event when the initialization of a part of magnets is required.
- Change signal from T clock to B clock
- Change signal from B clock to T clock

2-4. Looked-Up Table

LUT is a memory to convert any data placed on the address line to another data immediately. This feature is useful to convert an accounted value of B clock to the rf frequency which is not always linear. 80k steps of table is required when BM is excited up to 1.6T at B clock of 0.2G. Then dual 80k x 20-bit memory is provided, of which one serves to make data output and the other receives next data simultaneously.

2-5. Software functions of DPO

1) SH-1 CPU for control
   - Communication with Host CPU of IOC on VMEbus
   - Communication with SH-2 CPU for calculation
   - Execution of event signal
   - VMEbus and VSBbus control
   - Initialization and placing data on LUT
   - Smoothing control of pattern
   - Data output synchronized with external clock
2) SH-2 CPU for calculation
   - Communication with SH-1 CPU for control
   - Calculation of feed-back control or data filtering
   - Smoothing calculation of pattern

3. CURRENT STATUS AND DISCUSSION

DPO with basic firmware will be prepared for performance test by the end of this year. DPO will also provide a function of timing pattern generator which produces dynamically various event control timings. System considerations, such as pattern data-base construction and management, division of tasks among host computer and DPI/DPO, are necessary to specify further details and to establish the best way of usage.

High-speed digital feed-back control with high

accuracy is attractive to challenge many technical matters of instabilities in various synchrotron operation. We expect that the combination of DPI/DPO will be useful to reduce beam ripple or to stabilize beam position by means of high-speed data acquisition and processing.

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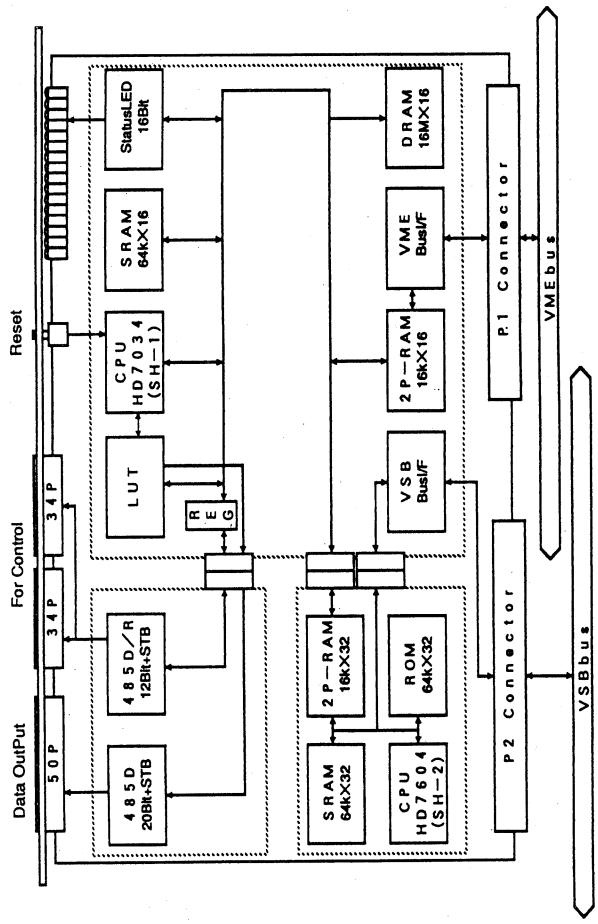

Fig.1 Block Diagram of DPO

TABLE 1 Outline Specification of DPO

	Main Board	Mezzanine Board for calculation	Mezzanine Board for I/O adaptation
CPU	SH7034(SH-1) • 4kB On-chip RAM • 64kB On-chip ROM • Hardware multiplier • 9ch. Ext. interrupt handler • 4ch. DMA controller • 5ch. Timer/Counter • 16bit Timing pattern gen. • Watch-dog timer • 2ch. Serial comm. port • Universal I/O ports	SH7604(SH-2) • 4kB cache memory • Hardware multiplier • Hardware divider • 15ch. Ext. interrupt handler • 2ch. DMA controller • 16bit Counter • Watch-dog timer • 1ch. Serial comm. port	Two 16bit bi-directional control signal port with strobe (Opto-isolated RS485 interface) 20bit+Strobe output port (Opto-isolated RS485 interface)
Clock	20MHz (16MIPS)	28.7MHz (25MIPS)	
SRAM	128kB with zero wait state	256kB with zero wait state	
DRAM	16MB with zero wait state	-	
Dual-ported SRAM	32kB with one clock wait state	64kB with one clock wait state	
LUT SRAM	384kB with 20bit U/D counter	-	
Front panel functions	16bit Status LED Reset switch	-	
Bus spec.	VMEbus IEC821 compatible slave interface (A24,D16) VSBbus IEC821 compatible master/slave interface		
Operating condition	Power source: 5V±5% , typ. 3A 5V±10%, typ.1.5A (I/O isolation p/s supplied from front connector) Temperature : 0℃~50℃ Humidity : 30%~90% (Non-condensing)		