MULTI-HARMONIC RF ACCELERATION SYSTEM FOR MEDICAL PROTON SYNCHROTRON

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Abstract

We have been developing an RF acceleration system for medical proton synchrotron. In order to reduce the beam loss by space-charge effect in a low energy domain, the multi-harmonic RF acceleration method is effective, in which the second and the third harmonic signals are superposed on the fundamental signal. We have applied the high-speed digital signal processing technique developed originally, to fulfill real-time feedback control of the frequency, phase and amplitude of the second and the third harmonic signals as well as the fundamental signal.

1 INTRODUCTION

We have supplied the proton synchrotron system to the Wakasa-wan Energy Research Center (WERC) and the Proton Medical Research Center (PMRC) at the University of Tsukuba. As for the accelerator system for proton therapy, simple control and stable beam supply are demanded because of a few operators. Therefore, we have developed the FINEMET® core loaded type un-tuned RF cavity and the RF digital control system using a direct digital synthesizer [1]. These equipments can generate a high voltage and realize simple frequency control.

The accelerator system, which we have been developing, is a small synchrotron system with low energy beam injection. Generally, in the low energy domain, the beam loss by the space-charge effect is expected. In order to reduce this beam loss, "multi-harmonic RF acceleration" is effective. The multi-harmonic RF acceleration is the method to mitigate the space-charge effect by keeping peak beam density low. The harmonic signals with the integral multiple frequencies of the fundamental signal are superposed on RF acceleration voltage, and the resulting bunched beam waveform is flattened.

It is important to control the phase and amplitude of the harmonic signals relative to the fundamental signal, in order to carry out the multi-harmonic RF acceleration. Therefore, the high-speed digital signal processing system that can realize the multi-harmonic RF acceleration is under development.

2 SYSTEM OVERVIEW

Figure 1 shows the block diagram of the present RF acceleration system. The RF acceleration system consists of five sub-systems: B-clock system, analog control system, digital control system, RF amplifier and RF cavity.

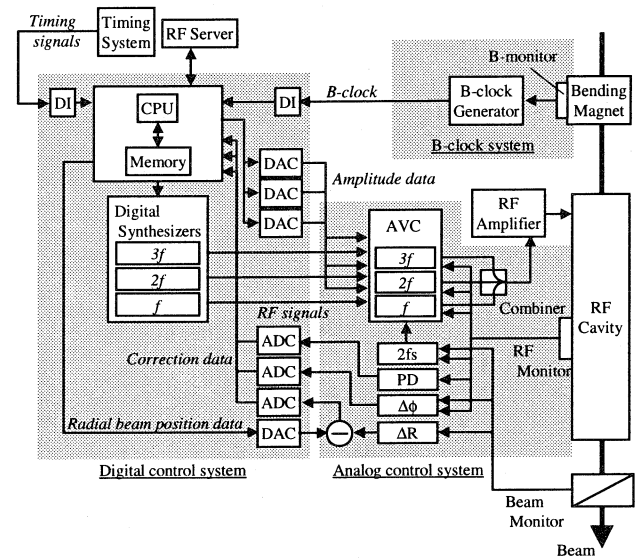

Figure 1:Block diagram of the present RF acceleration system

The B-clock signal based on the output signal from the B-monitor, which detects change of magnetic field intensity, is outputted by the B-clock system, and it is transmitted to the digital control system. The maximum clock-rate is 100kHz, corresponding to a 0.2 gauss increase. The analog control system has five feedback loops: Automatic Voltage Control loop (AVC), radial beam position control loop (ΔR loop), two kinds of synchrotron-oscillation suppression loops (Δφ and 2fs loop), and phase-difference detection loop (PD). The digital control system updates the fundamental RF frequency data by the B-clock signal. And the digital control system carries out feedback operation by the frequency correction data from the analog signal processing system. The frequencies of the harmonic signals are obtained by carrying out the integral multiple of the feedback operation result. These operations have to be processed in less than 2μs [2]. In the digital control system, the phase feedback operation of the output RF signal and the amplitude control are processed in parallel with these frequency controls. The above operation results are set on the digital synthesizers, respectively. The fundamental signal and the harmonic signals are combined after amplitude control by the analog control system. The combined signal is amplified with the RF

amplifier, and fed to the RF cavity. As shown above, the digital control system has to control the frequencies, phases, and amplitudes of the fundamental and harmonic signals on real-time. We have applied "SRC (Super Real-time Controller)" to the multi-harmonic RF acceleration system in order to realize the above-mentioned real-time control. The original SRC was developed for the intelligent robot control system [3] in which both high-speed I/O processing and complicated operation processing were demanded.

3 SUPER REAL-TIME CONTROLLER

Figure 2 shows the block diagram of the digital control system adopting the SRC, and Table 1 shows the specifications of the digital control system.

From viewpoint in processing the SRC is divided into two independent parallel control systems, that is, motion control system and intelligent control system, in order to attain a real-time performance. Furthermore, the SRC has the shared memory system (Dual Port RAM system, DPR) that can be accessed from the intelligent control system and the motion control system. A PC for communication control (RF Server) can also access to DPR via communication interface (COM I/F). The COM I/F has the data transmission capability of more than 11Mbps. The DPR makes transfer of data possible is in the mutual processing system.

The hardware unit of the SRC consists of base processor and I/O units. The base processor unit is provided with CPU and memory for the motion control and intelligent control system, respectively. In this system, the CPU of the base processor unit carries out a setup and initialization of pattern or constant data that are transmitted from the RF-server to the I/O unit. Processing of real-time control is carried out by FPGA unit prepared for the I/O unit.

The I/O unit has I/O interface for each control system, and the I/O interface connects to the FPGA unit. The motion control system processes the frequency control in which the high-speed feedback less than 2μs is required. The intelligent control system processes the phase and amplitude control in which many I/O control and complicated processing less than 10μs are required.

Table 1: Specifications of the RF digital control system

Frequency Range	0.5-10 MHz
Frequency Resolution	24 bits (4.2Hz/LSB)
Phase Resolution	12 bits (0.08deg/LSB)
Amplitude Resolution	12 bits (0.37V/LSB)
Pattern Memory Capacity	16 Mbytes (SRAM)
System Clock Frequency	140 MHz (double edge)
Synthesizer Clock Frequency	70 MHz

An FPGA unit is divided into the three control blocks, that is, the frequency controller, phase and amplitude controller and memory controller. Each controller has particular FPGAs. The frequency controller performs the fundamental frequency feedback, the calculation of the second and the third harmonics frequencies and RF signals output management. The phase and amplitude controller processes the phases of the second and third harmonic signals and the amplitudes of the fundamental and harmonics signals. The memory controller manages the pattern data address by the B-clock signal and T-clock signal.

The I/O and the base processor units are connected through Direct Access Channel (DA Ch.) in order to realize high-speed data transmission. In the SRC, the same simple and high-speed processing as memory access is realized for data transfer with the I/O interface. The pattern and constant data that are used for RF

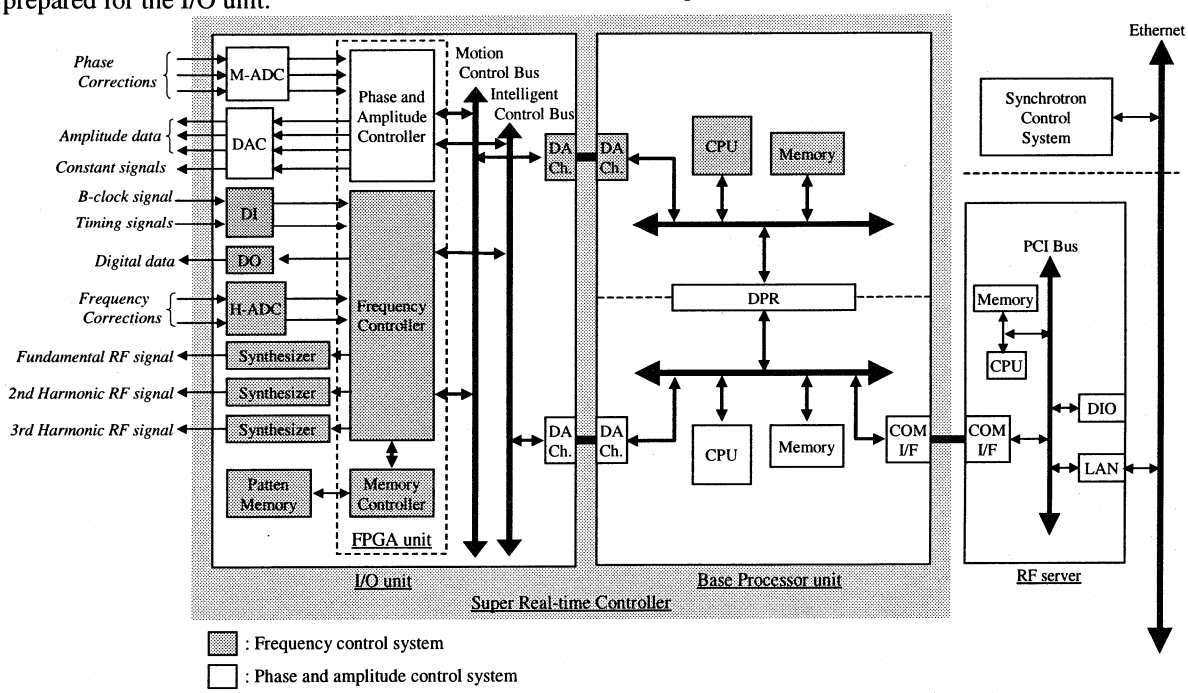

Figure 2 : Block diagram of the digital control system in the RF aceleration system

acceleration are set up from a synchrotron control system via Ethernet. Those data are received with the RF Server, and transmitted to the SRC via COM I/F. The pattern data transmitted from the RF Server is saved in the memory (16MByte) on I/O unit, and the constant data are saved at constant register on the FPGA unit.

3.1 Frequency Control

The frequency of the digital synthesizer is calculated as follows. The frequency correction voltages (ΔR and $\Delta\phi$) are sampled at a high-speed ADC (H-ADC). The frequency correction voltages are converted into the frequency correction data, which are added to the frequency data of the fundamental signal updated by the B-clock signal. The second and third harmonic frequency data are calculated based on the fundamental frequency, respectively.

It is necessary to reduce an error of the setting frequency of the digital synthesizer between the multiple RF signals. In order to suppress the error of the frequency data between the digital synthesizers low, frequency resolution of the digital synthesizer must be high. By expressing frequency data in 24 bits, the accuracy of 4.2Hz/LSB is acquired by a control clock of 70MHz.

3.2 Amplitude Control

It is necessary to superpose the harmonic signals to the fundamental signal at the desired amplitude rate. The amplitude values are prepared beforehand for the fundamental signal and the harmonic signals by pattern data. The amplitude values are updated with the control clock (T-clock) in a cycle of 50kHz and set to the AVC circuit during acceleration control. The AVC circuit is equipped for each frequency component to realize the desired amplitude values.

3.3 Phase Control

The phase of the harmonic signals must follow change of the synchronous-phase of the fundamental signal. This synchronous-phase is determined from the amplitude value of the fundamental signal and the rate of change of magnetic field strength. The amplitude value of the fundamental signal is controlled by the T-clock signal. The phase data of the harmonic signals are also beforehand prepared by pattern data and are updated by the T-clock signal.

Moreover, in order to obtain the desired bunched beam waveform, it is necessary to suppress the phase error of the fundamental and harmonic signals below into ±1degree. The output phase error between RF signals is caused by a difference of the output timing between the digital synthesizers. Furthermore, the output signal from a digital synthesizer is delayed with the individual difference of the analog circuit. The maximum frequency of the fundamental signal that can be combined with the second and the third harmonic signals is 3.3MHz because of the upper limitation of the operation frequency range of the RF acceleration system. The phase error of ±1degree at the frequency of this fundamental signal is converted into time of less than 1ns. Therefore, an error of even one control clock for output timing is not allowed. For a constant error like the output phase delay between the multiple RF signals, the frequency characteristic of a RF circuit is measured and the frequency-dependent correction data based on the measurement are beforehand prepared on pattern data. The frequency-dependent correction data of the fundamental and harmonic signals are update by the B-clock signal. For an inconstant error like a temperature drift, choosing a circuit element with the sufficient temperature characteristic is essential.

As shown above, phase control of the harmonic signals needs to add the data updated with the two different asynchronous control clocks one by one, and needs to set the data on the digital synthesizers. In this system, by phase and amplitude controller, the two control pattern data are updated asynchronously, and addition operation is carried out one by one. Furthermore, phase feedback operation is carried out by phase-difference detection data extracted by medium-speed ADC. By the phase feedback operation, stable formation of optimal bunch waveform is attained, even when the frequency characteristic of the RF acceleration system changes.

4 SUMMARIES

We have been developing an RF digital control system realizing the multi-harmonic RF acceleration to reduce the beam loss by the space-charge effect in the low energy domain. It is necessary that the frequency, phase, and amplitude of the fundamental signal and the harmonic signals to be controlled on real-time.

In order to realize these real-time controls, we have applied our original "SRC (Super Real-time Controller)" to this system. The SRC consists of the motion control system for frequency control and the intelligent control system for the phase and amplitude control. Processing of real-time control is carried out by FPGA

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