CSNS Timing System

G. Lei

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CSNS
CHINESE ACADEMY OF SCIENCES

Contents of this talk

- Breif introduction to CSNS
- Requirement investigation
- Strategy: based on event timing concept
- Progress
- Challenges

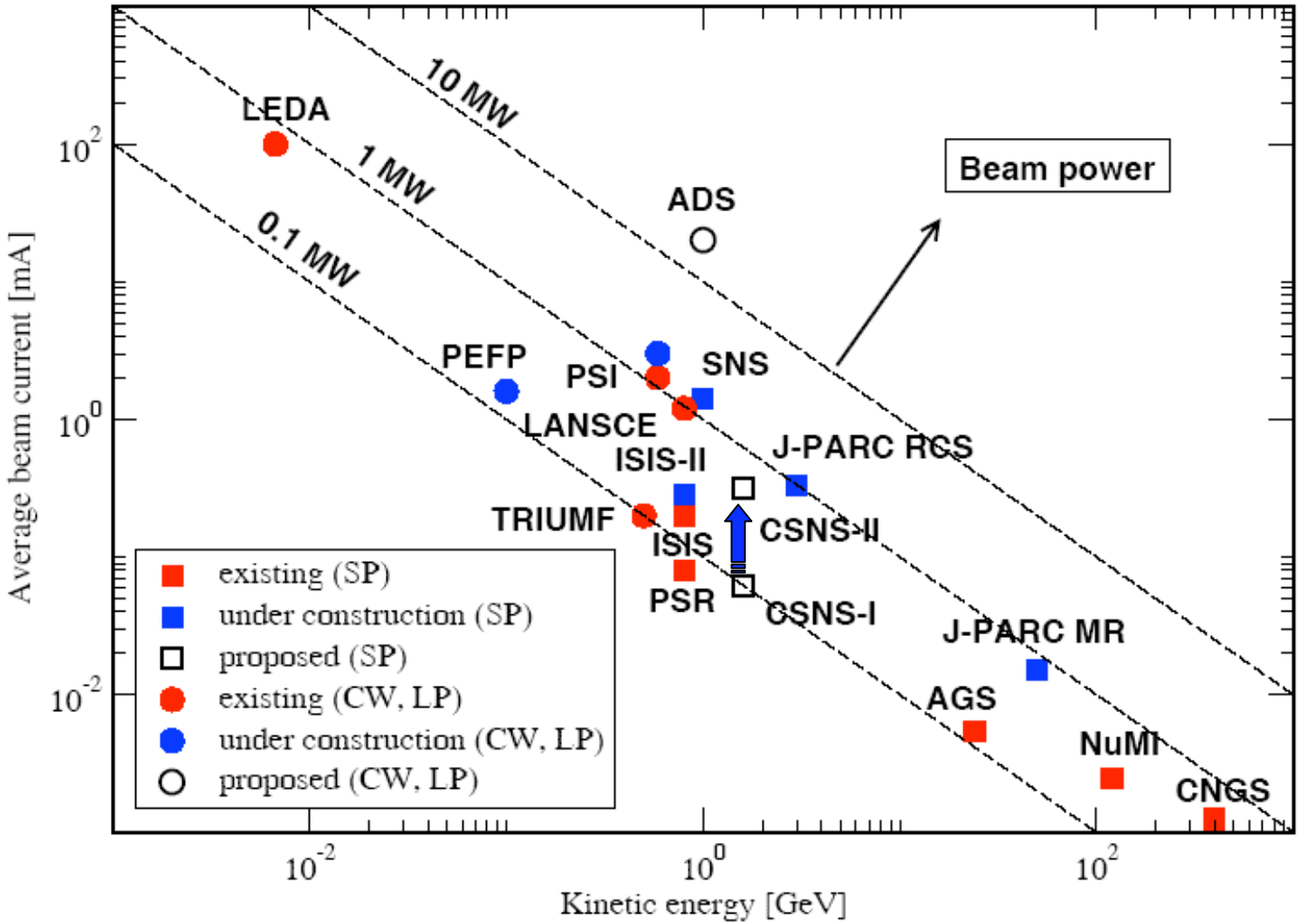
中国散裂中子源


北京市
North Korea
三明市
福州市
赣州市
梅州市
龙岩市
莆田市
泉州市
新竹市
漳州市
厦门市
台中市
韶关市
清远市
河源市
汕头市
嘉義市
广州市
肇庆市
东莞市
惠州市
佛山市
汕尾市
台南市
中山市
深圳市
高雄市
Hong Kong
香港
江门市
Macau
澳門

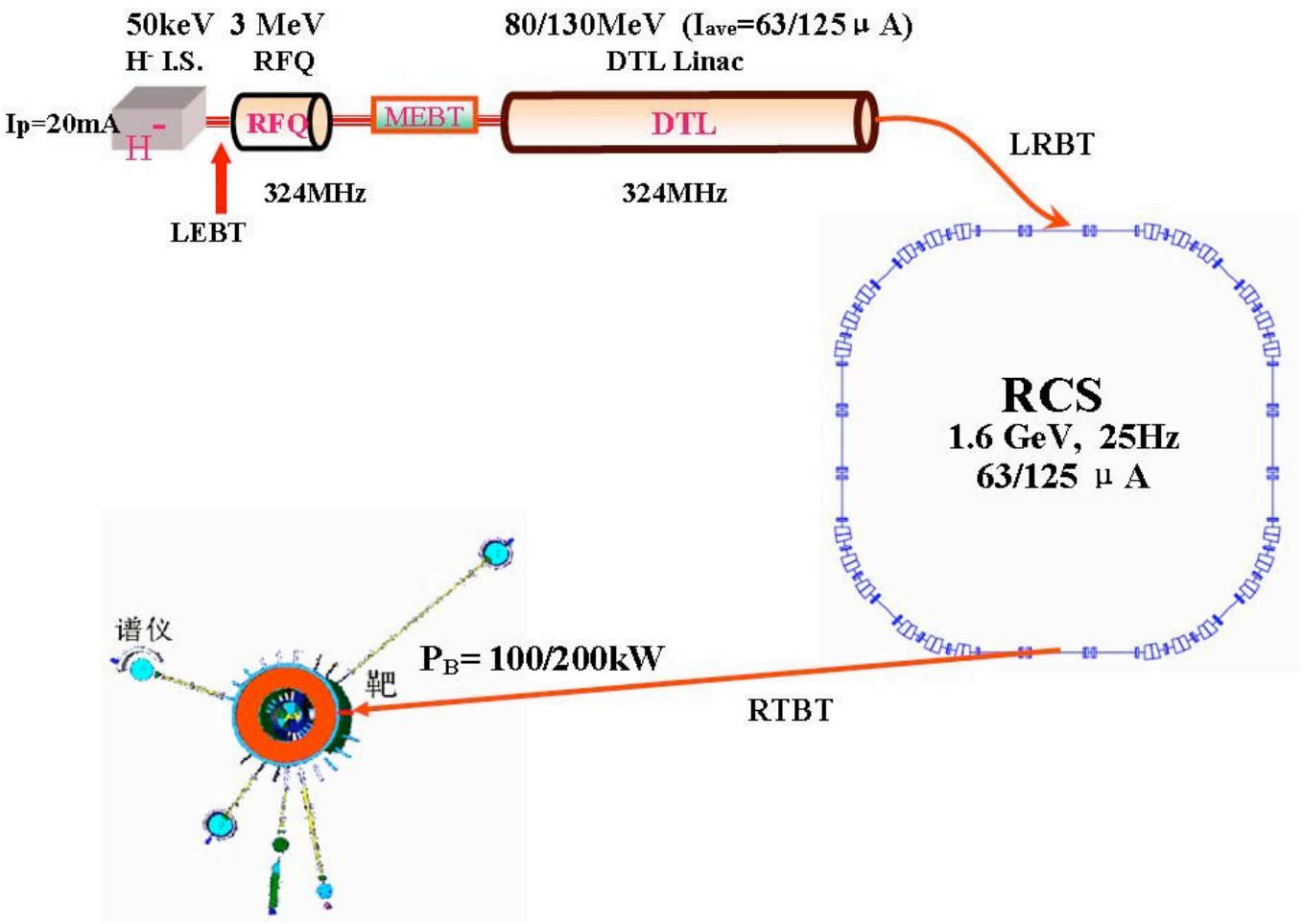
Layout design based on the geology detection last year

Accelerator beam power front

Jie Wei



中国散裂中子源

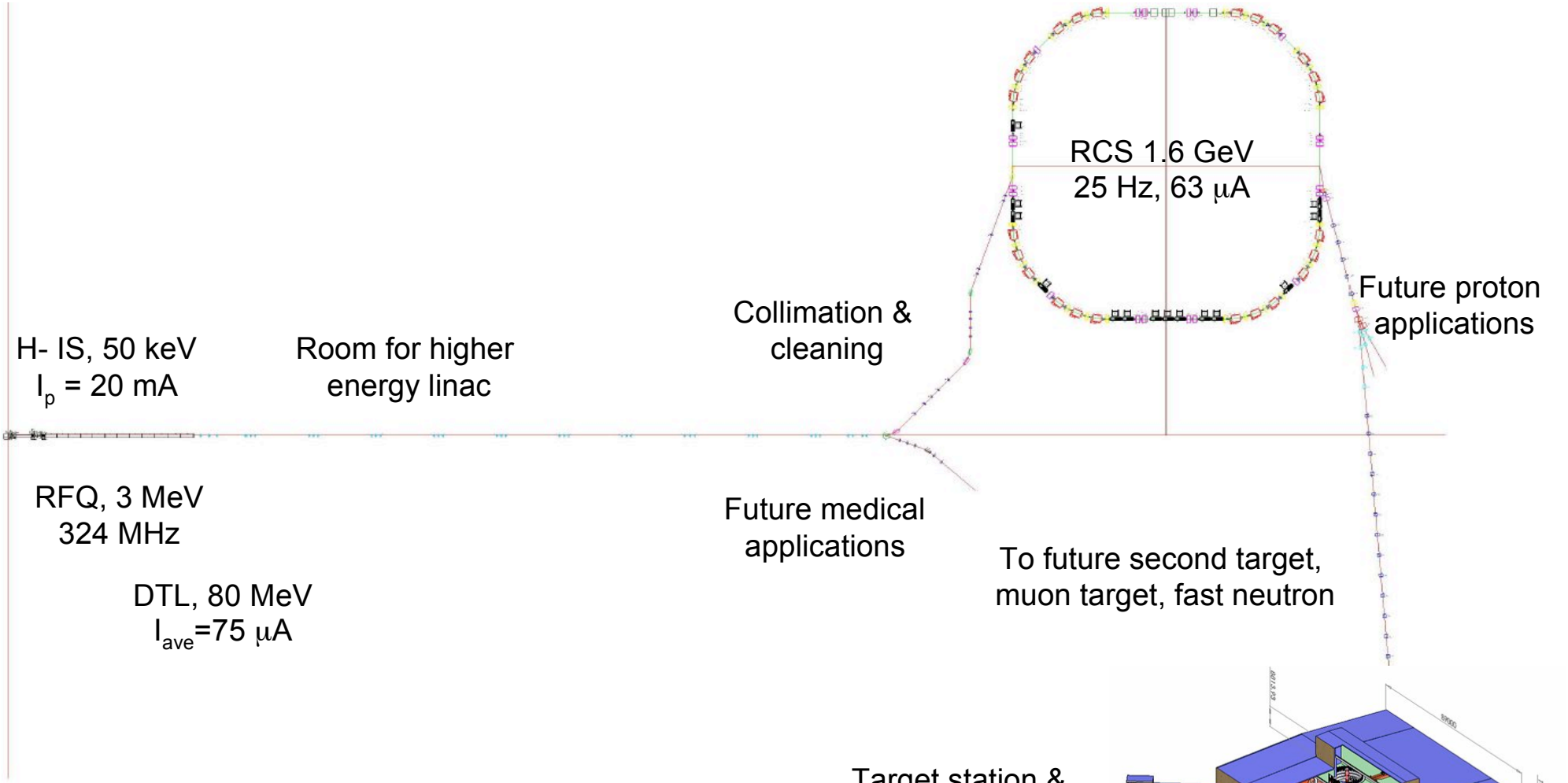


Beam Travel Length

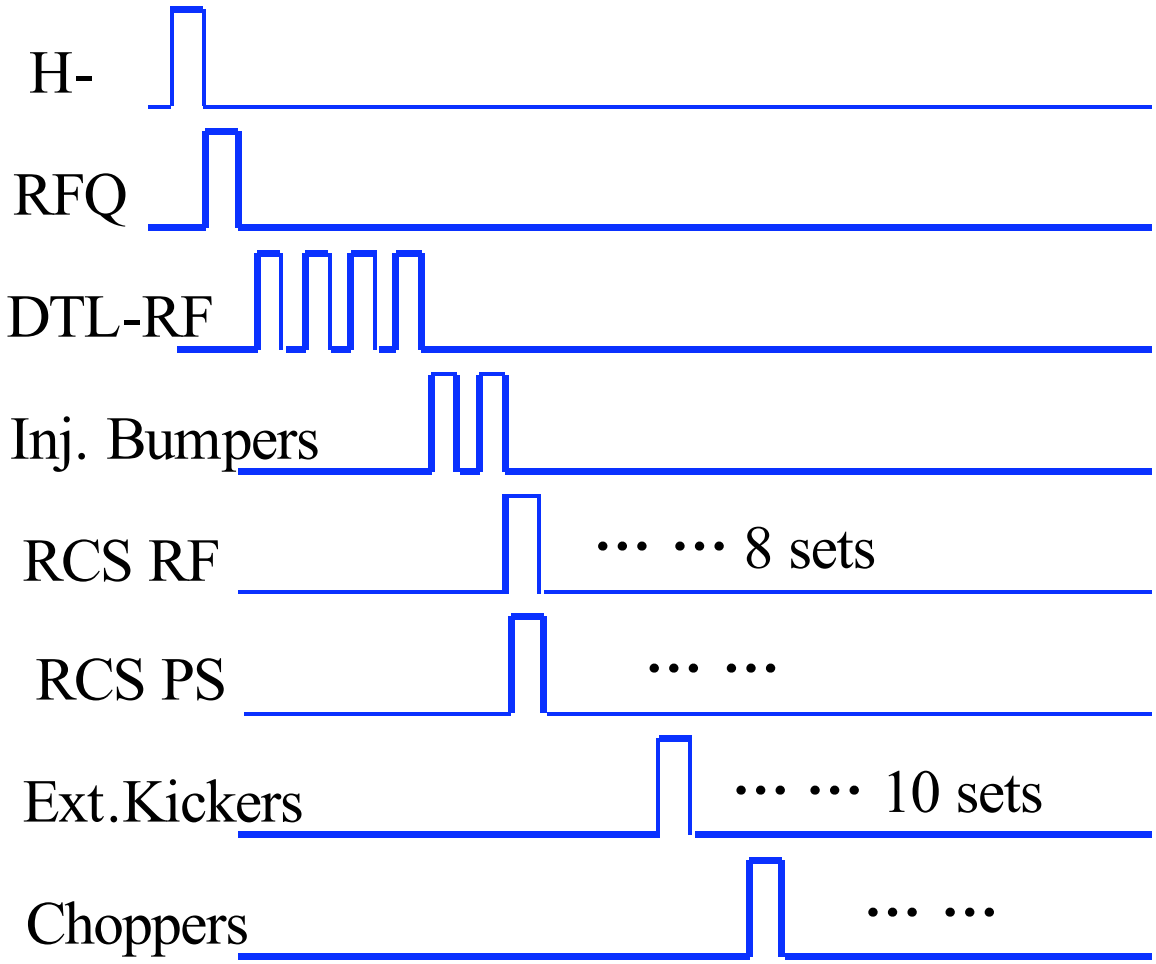
FE	9m
DTL	38.13m
LRBT	170.5m
RSC	238.8m
RTBT	123m

CSNS baseline layout 一期规划

Jie Wei



Requirement investigation



CSNS timing task (1)

- **Scheduled timing**
  - H- source
  - magnet power supply,
  - injection bumpers and extraction kickers
  - beam diagnostics
  - Linac and RCS RF
  - Target and detectors

CSNS timing task (2)

- **Synchronized timing**
  - **Triggers to LEBT /MEBT chopping should be synchronized with RCS RF phase**
  - **Triggers to extraction kickers should be synchronized with RCS beam**

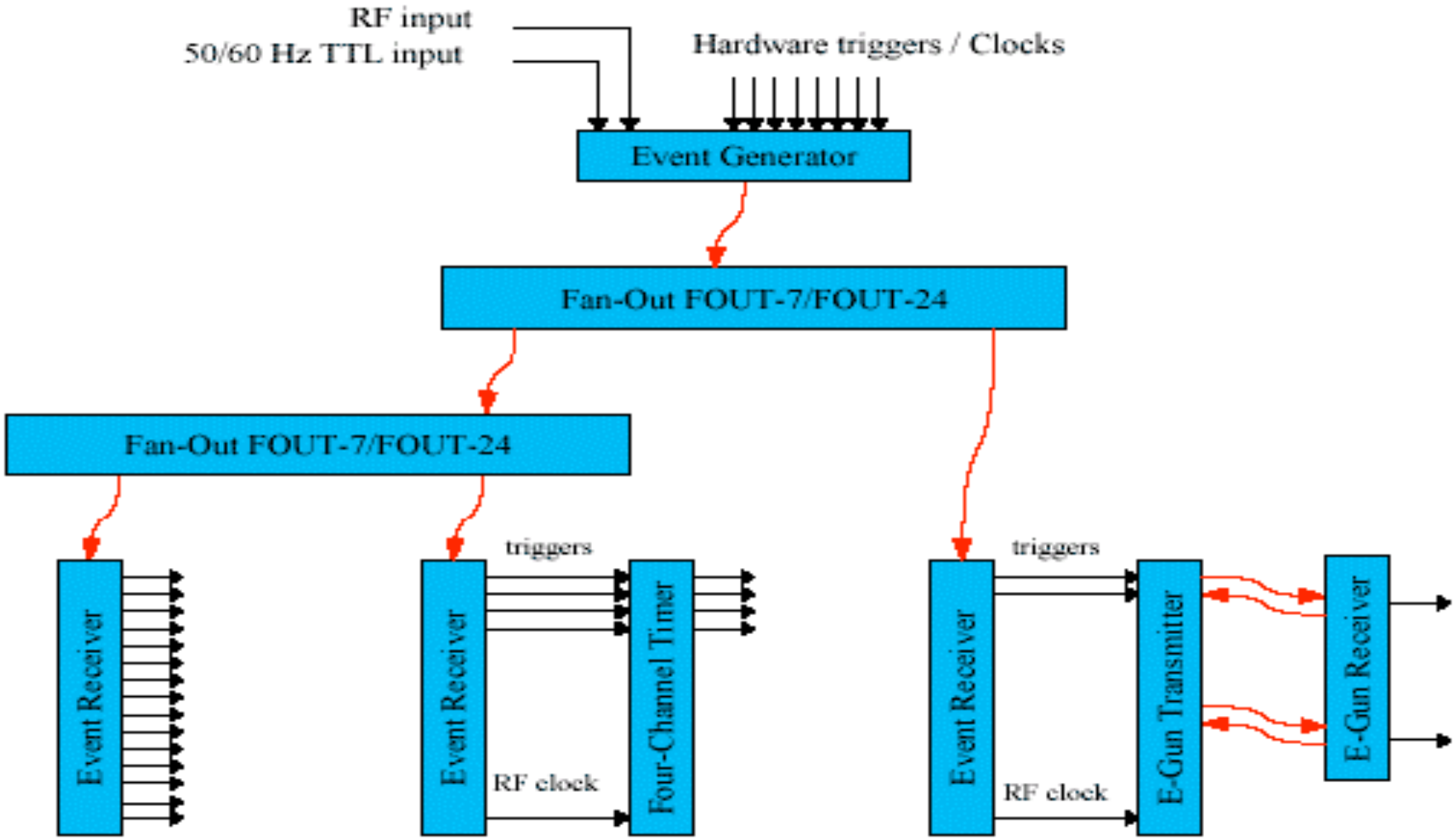
CSNS timing task (3)

- **Synchronizing clock**
  - 1MHz clock for magnet power supply
- **RF reference distribution**
  - to linac LLRF and BI
- **Timestamp and some operating related parameters distributed through dedicated event timing links**

Requirement for triggers

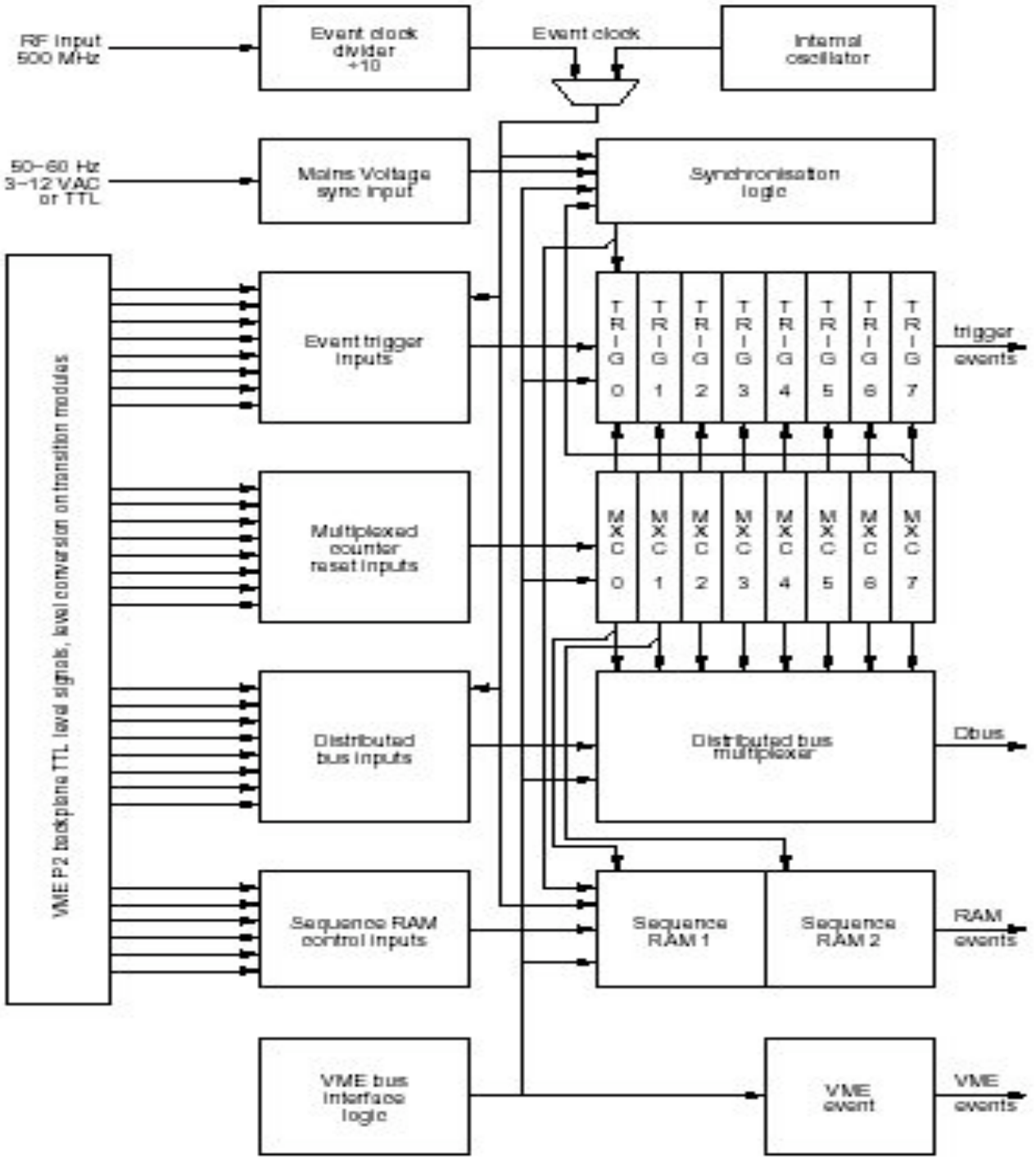
sys	device	num	delay Ch	pulse width	Max. Freq	rising time	jitter (RMS)	delay scope	adjust step
PS	DTL-Q	76	76	10us	25Hz	<10ns	<100ns	<40us	100ns
	RCS-B	1	1	10us	25Hz	<10ns	<100ns	<40us	100ns
	RCS-Q	7		10us	25Hz	<10ns	<100ns	<40us	100ns
	RCS-C	72		10us	25Hz	<10ns	<100ns	<40us	100ns
RCS RF	LLRF	14	14	1us	25Hz	<10ns	<100ns	<40us	100ns
Inj. Ext.	bumper	2	2	1us	50Hz	5ns	1ns	1ms	5ns
	kicker	10	10	1us	50Hz	5ns	1ns	1ms	5ns
Target	chopper	9	9	50us	25Hz	1us	1us	<40us	100ns
linac LLRF	sys start	9	9	5us	25Hz	<10ns	<100ns	<40us	100ns
	RF GATE	9	9	200us ~ 800us	25Hz	<10ns	<100ns	<40us	100ns
	mod gate	9	9	500us ~ 1ms	25Hz	<10ns	<100ns	<40us	100ns
H- source	H_2 PS	3	3	300us	25Hz	<10ns	<100ns	<40us	100ns
	Arc PS	3	3	800us	25Hz	<10ns	<100ns	<40us	100ns
	Ext. PS	3	3	500us	25Hz	<10ns	<100ns	<40us	100ns
BI		333	333		25Hz	<10ns	<100ns	<40us	100ns

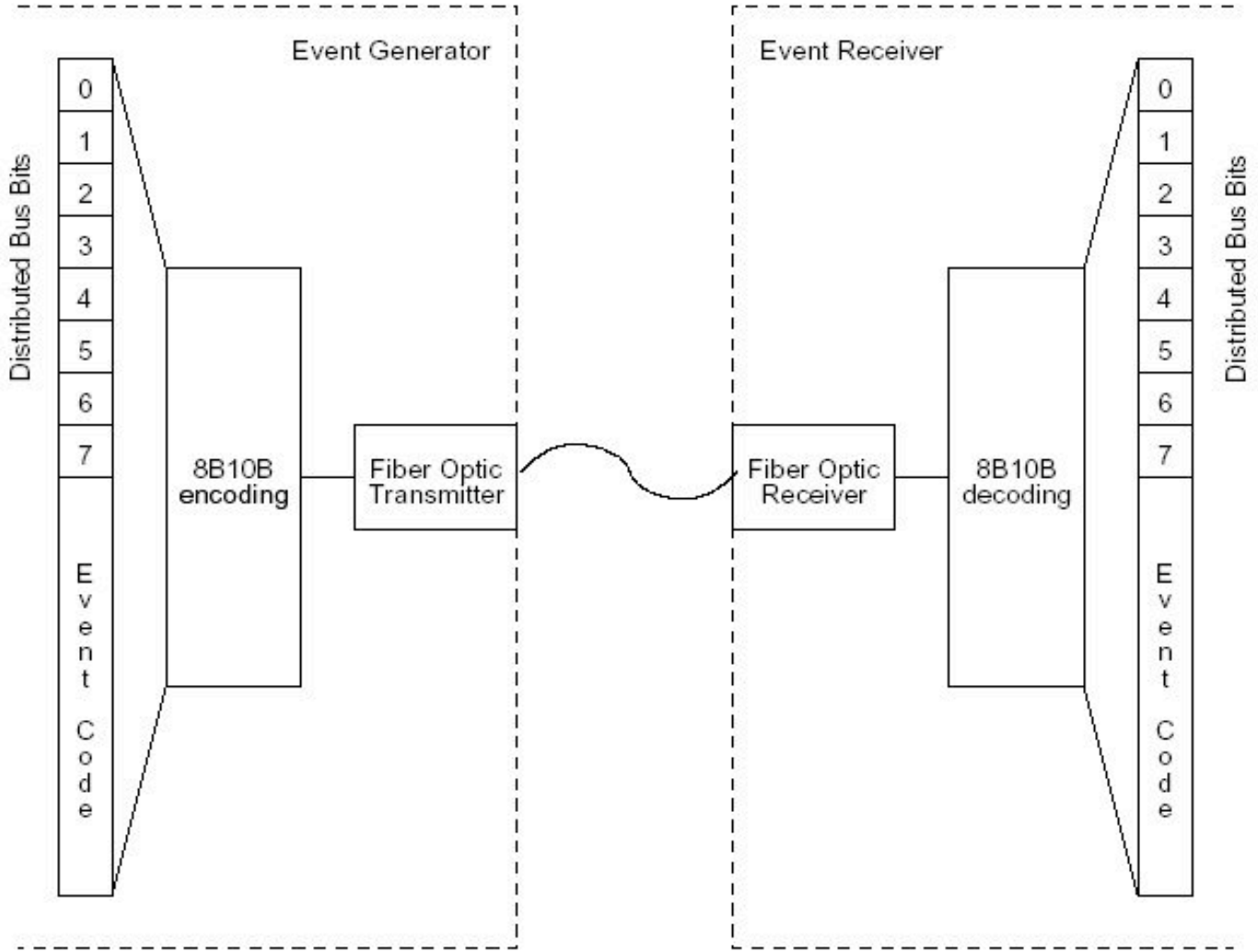
Strategy: adopting event timing concept



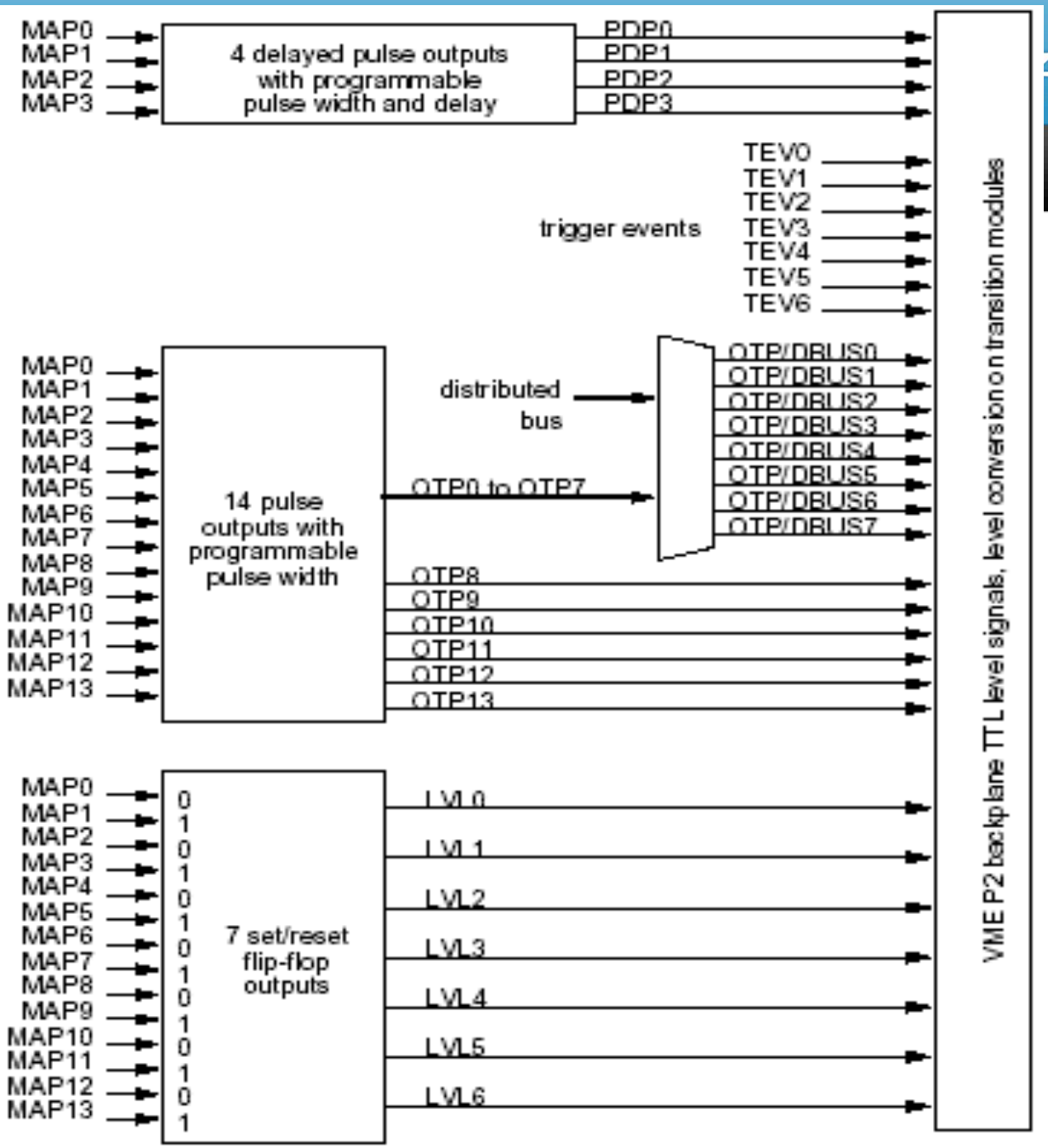
Event timing system Jukka

- Functionality based on the APS timing system
- Redesigned for SLS → Series 100
- Improved performance for Diamond → Series 200
- Timing signals needed for synchronisation of subsystems are applied to Event Generator (EVG) or generated by EVG
- Timing information is converted to 8-bit event codes and disbtributed to Event Receivers (EVR) as optical signals
- Event clock rate determines timing resolution:
  - Minimum clock rate 50 MHz, 20 ns resolution
  - Maximum clock rate 125 MHz, 8 ns resolution
- 8-bit distributed bus running in parallel and independent of timing events allows distribution of eight signals updated with the event clock rate


RF Input
500 MHz
Event clock divider ÷10
Event clock
Internal oscillator
50–60 Hz
3–12 VAC
or TTL
Mains Voltage sync input
Synchronisation logic
VME P2 backplane TTL level signals, level conversion on transition modules
Event trigger inputs
TRIG 0
TRIG 1
TRIG 2
TRIG 3
TRIG 4
TRIG 5
TRIG 6
TRIG 7
trigger events
Multiplexed counter reset inputs
MXC 0
MXC 1
MXC 2
MXC 3
MXC 4
MXC 5
MXC 6
MXC 7
Distributed bus inputs
Distributed bus multiplexer
Dbus
Sequence RAM control inputs
Sequence RAM 1
Sequence RAM 2
RAM events
VME bus interface logic
VME event
VME events

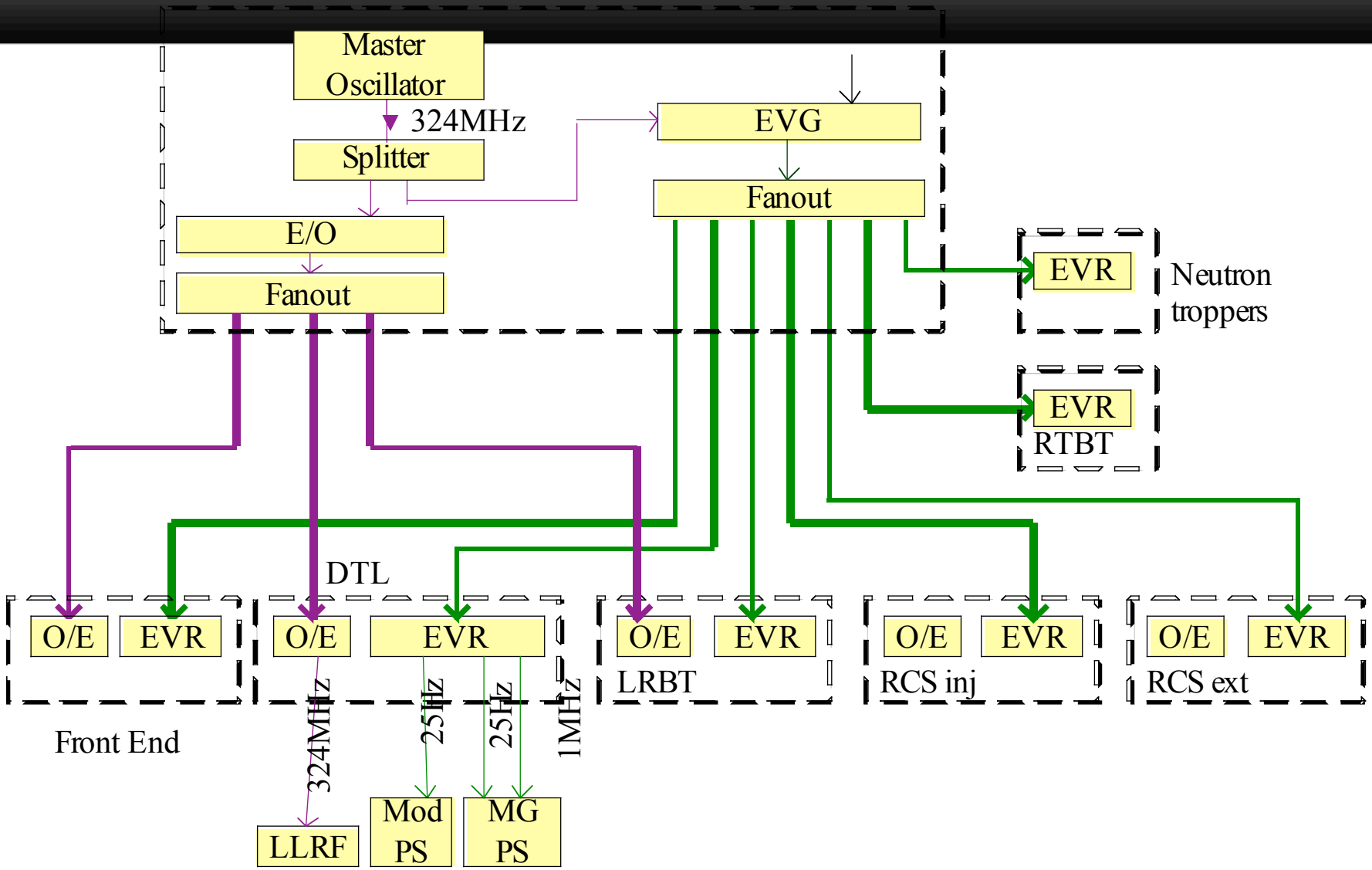

Event Generator
Event Receiver
Distributed Bus Bits
0
1
2
3
4
5
6
7
Event Code
8B10B encoding
Fiber Optic Transmitter
Fiber Optic Receiver
8B10B decoding
Distributed Bus Bits
0
1
2
3
4
5
6
7
Event Code

EVR


MAP0
MAP1
MAP2
MAP3
4 delayed pulse outputs with programmable pulse width and delay
PDP0
PDP1
PDP2
PDP3
TEV0
TEV1
TEV2
TEV3
TEV4
TEV5
TEV6
trigger events
MAP0
MAP1
MAP2
MAP3
MAP4
MAP5
MAP6
MAP7
MAP8
MAP9
MAP10
MAP11
MAP12
MAP13
14 pulse outputs with programmable pulse width
distributed bus
OTP0 to OTP7
OTP/DBUS0
OTP/DBUS1
OTP/DBUS2
OTP/DBUS3
OTP/DBUS4
OTP/DBUS5
OTP/DBUS6
OTP/DBUS7
OTP8
OTP9
OTP10
OTP11
OTP12
OTP13
MAP0
MAP1
MAP2
MAP3
MAP4
MAP5
MAP6
MAP7
MAP8
MAP9
MAP10
MAP11
MAP12
MAP13
0 1 0 1 0 1 0 1 0 1 0 1 0 1
7 set/reset flip-flop outputs
LVL0
LVL1
LVL2
LVL3
LVL4
LVL5
LVL6
VME P2 backplane TTL level signals, level conversion on transition modules

Strategy: adopting event timing concept

- Event Generator (EVG), Event Receiver (EVR)
- Multi-mode optical fiber between EVG and Fanout/EVR
- 8 bit event codes and 8 clock
- Timestamp and data buffer
- Heartbeat monitor
- Interlock input to disable some outputs
- Fine grained adjustable output pulses and clock frequencies.


Master Oscillator
324MHz
Splitter
E/O
Fanout
EVG
Fanout
EVR
Neutron troppers
EVR
RTBT
DTL
O/E
EVR
O/E
EVR
O/E
EVR
O/E
EVR
O/E
EVR
LRBT
RCS inj
RCS ext
Front End
324MHz
25Hz
25Hz
1MHz
LLRF
Mod PS
MG PS

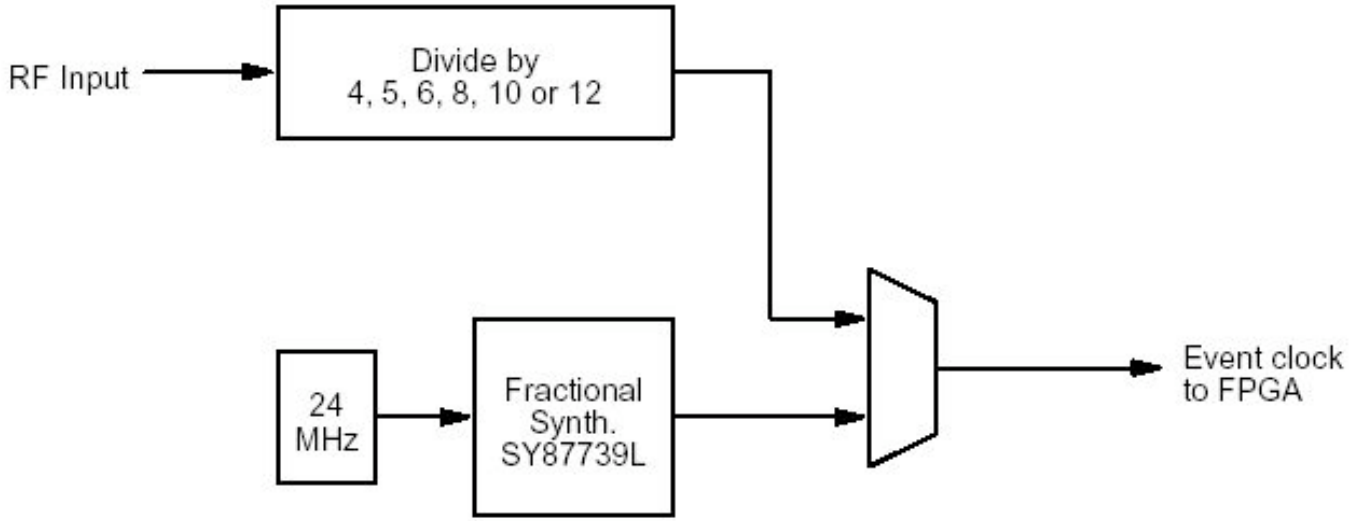
Design the CSNS timing system using EVG/EVR

Using experience of BEPCII timing system, but requirements different

- **Decide the event clock**
  - **324MHz/4 = 81MHz**
- Calculate the parameters for Fractional-N synthesizer
  - Work out several equations and inequalities

Fractional Synthesiser

- **A Micrel (http://www.micrel.com) SY87739L Protocol Transparent Fractional-N Synthesiser with a reference clock of 24 MHz is used in EVG. By correctly setting the parameters in this circuit, we can get proper frequency for CSNS timing system.**



Calculate parameters of Fractional-N synthesizer

f_{VCO} (min) = 540MHz, f_{VCO} (max) = 729MHz

$$f_{FNOUT} = \left[P - \frac{Q_{P-1}}{Q_P + Q_{P-1}} \right] \times f_{REF}$$

$$f_{VCO}(\min) < f_{REF} \times \left\{ P - \left[\frac{Q_{P-1}}{(Q_{P-1} + Q_P)} \right] \right\} < f_{VCO}(\max)$$

$$540\text{MHz} \le f_{WROUT} = \frac{N}{M} \times f_{FNOUT} = \frac{N}{M} \times \left[P - \frac{Q_{P-1}}{Q_{P-1} + Q_P} \right]$$

$$\times f_{REF} \le 729\text{MHz}$$

Calculate parameters of Fractional-N synthesizer

- f_{ref}=24MHz, event clock=81MHz
- $24 * (P - Q_{p-1}/(Q_{p-1} + Q_p)) / PostDivSel = 81$,

  $540 < 24 * (P - Q_{p-1}/(Q_{p-1} + Q_p)) < 729$,
- P=24, Q_{P-1}=3, Q_P=5, PostDivSel=7, N=M=14
- 0000 qp qpm1 divsel 000 PostDivSel NdivSel MdivSel

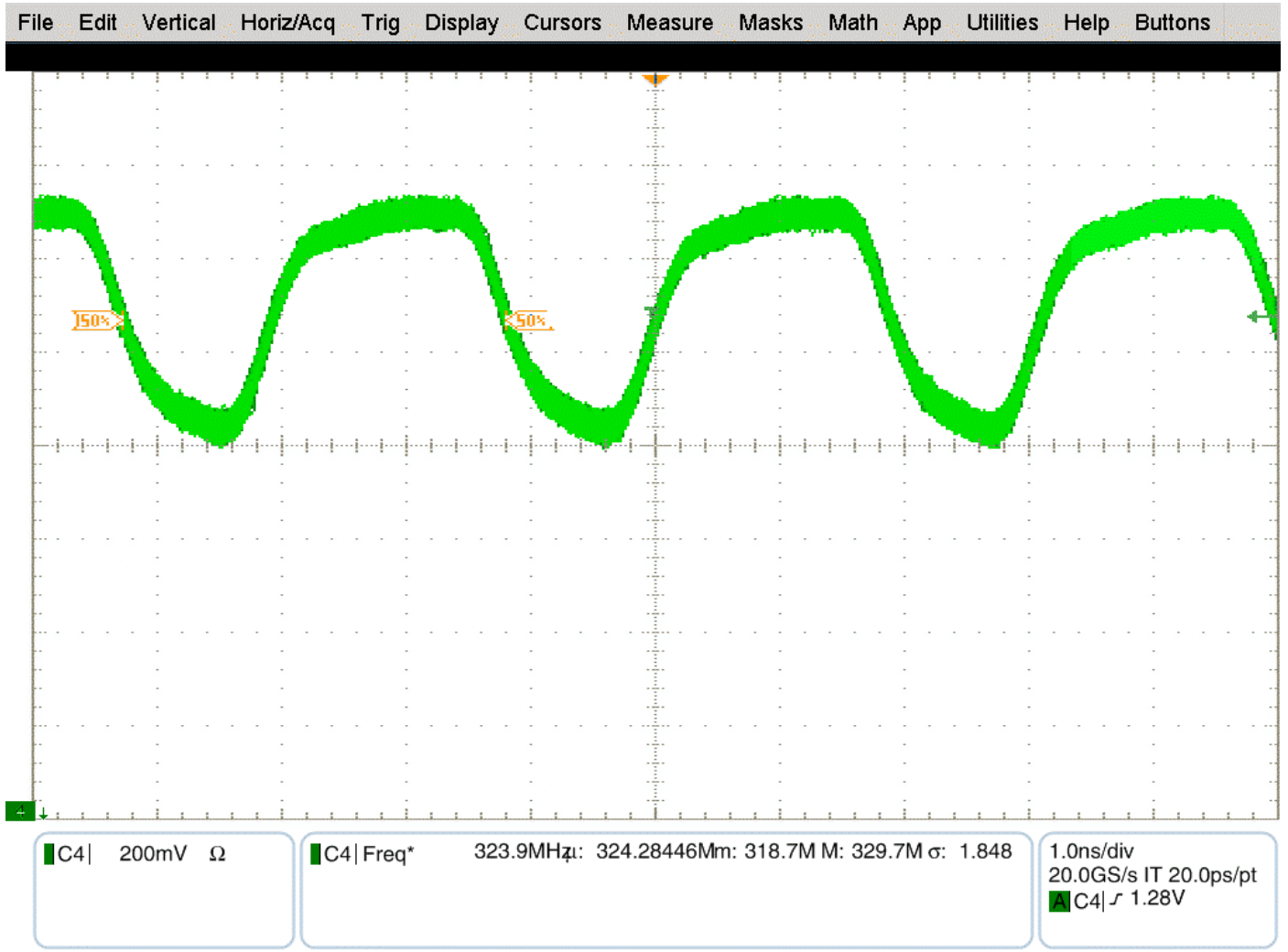
  0000 00101 00011 0111 000 00111 101 101

  = 0x028d c1ed

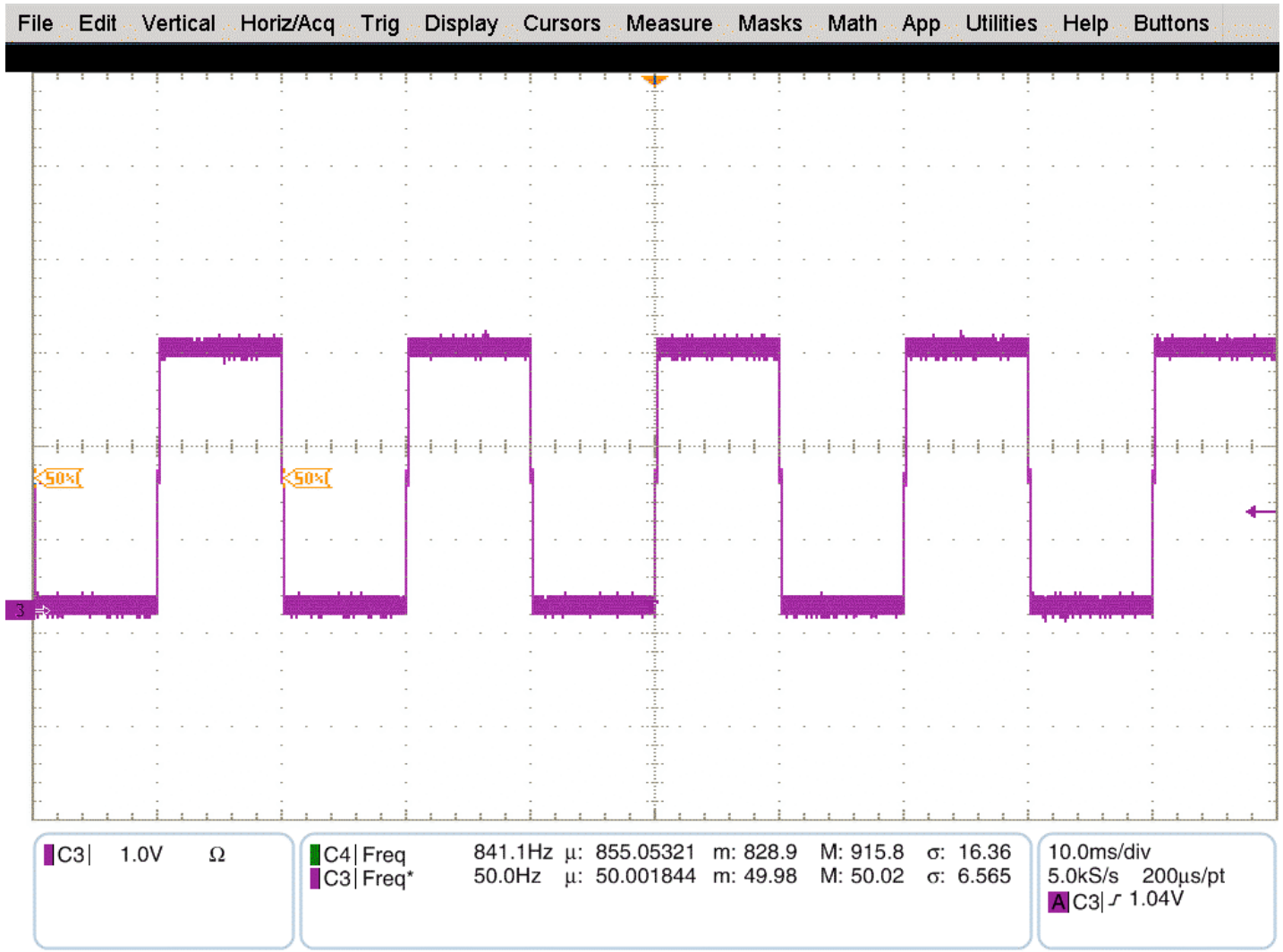
Progress (cont.)

- Very preliminary design
- Prototype 1
  - Got official approval
  - Hardware ordered but not reached us
  - Several experiments done using BEPCII spare parts

324MHz measured from EVR230, done by Guanglei Xu



50Hz (324MHz/4/1620000) generated from event clock in EVG, done by Guanglei Xu



Interlock design – using UNIV-TTL-IN

Challenges

- Interlock realization
- Synchronized timing
- Timestamp distribution by timing system to control system

Thank you all for your attention

Referenece (documents, discussions)

1. China Spallation Neutron Source, Jei Wei, etc.
2. Front End, Ouyang Huafu, 2007/5/1
3. Linac LLRF, LI Jian,etc.
4. Injection and Extraction, Tang Jingyu, Chi Yunong, Shen Li, etc.
5. CSNS Beam Diagnostics, Xu Taoguang
6. Discussions with Wang Sheng, Zhang Jing, etc.
7. EPICS Collaboration Meeting, ANL, Argonne, Jukka Pietarinen, Micro-Research Finland Oy.